

Features

- Low Offset Voltage: 40 μ V (Maximum)
- Input Offset Drift: 0.05 μ V/ $^{\circ}$ C
- High Gain Bandwidth Product: 350KHz
- Rail-to-Rail Input and Output • High Gain, CMRR, PSRR:130dB
- High Slew Rate: 0.17V/ μ s
- Low Noise: 1.6 μ Vp-p (0.01~10Hz)
- Low Power Consumption: 60 μ A /op amp
- Overload Recovery Time:6 μ s
- Low Supply Voltage: +2.5 V to +5.5 V
- No External Capacitors Required
- Extended Temperature: -40 $^{\circ}$ C to +125 $^{\circ}$ C

Application

- Temperature Sensors
- Medical/Industrial Instrumentation
- Pressure Sensors
- Battery-Powered Instrumentation
- Active Filtering
- Weight Scale Sensor
- Strain Gage Amplifiers
- Power Converter/Inverter

Description

The CBM8511, CBM8512, CBM8513, CBM8514(dual version & shutdown) series of CMOS operational amplifiers use auto-zero techniques to simultaneously provide very low offset voltage (40 μ V max) and near-zero drift over time and temperature. This family of amplifiers has ultralow noise, offset and power.

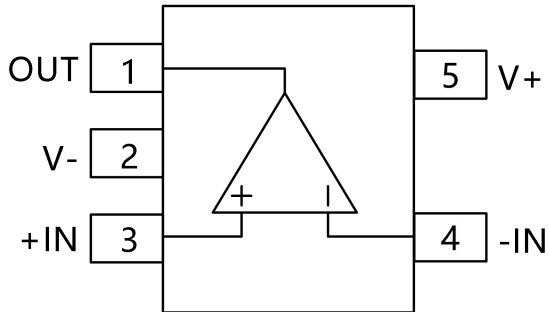
This miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 350KHz and slew rate of 0.17V/ μ s. Single or dual supplies as low as +2.5V(\pm 1.25V) and up to +5.5V (\pm 2.75V) may be used.

The CBM8511, CBM8512, CBM8513, CBM8514 (dual version with shutdown) are specified for the extended industrial and automotive temperature range (-40 $^{\circ}$ C to 125 $^{\circ}$ C). The CBM8511 single amplifier is available in 5-lead SOT23, 8-lead MSOP8 and 8-lead SOIC packages, The CBM8512 dual amplifier is available in 8-lead SOIC, 8-lead TDFN2x2 and 8-lead TSSOP narrow surface mount packages, The CBM8513(dual version with shutdown) comes in Micro-SIZE MSOP10. The CBM8514 quad is available in 14-lead SOIC and 14-lead narrow TSSOP packages.

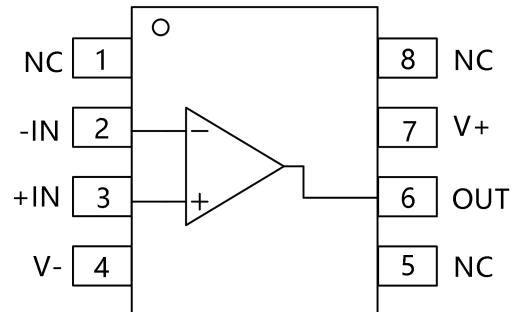
CATALOG

Features.....	
Application.....	
Description.....	
Pin Configurations.....	1
Electrical Characteristics.....	2
Typical Characteristics.....	5
Application Notes.....	8
Operating Voltage.....	8
CBM8513 Enable Function.....	8
Layout Guidelines.....	9
Package Outline Dimensions.....	10
SOT23-5.....	10
MSOP-8.....	11
MSOP-10.....	12
TSSOP-14.....	13
SOIC8(SOP8).....	14
SOIC-14(SOP14).....	15
Package/Ordering Information.....	16

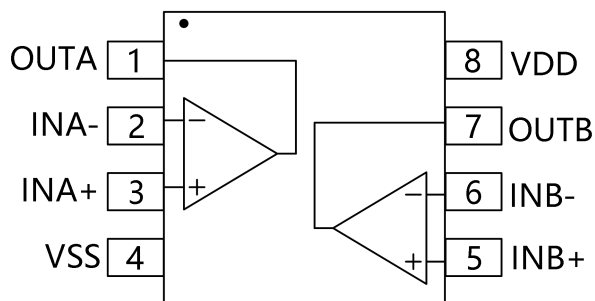
Pin Configurations



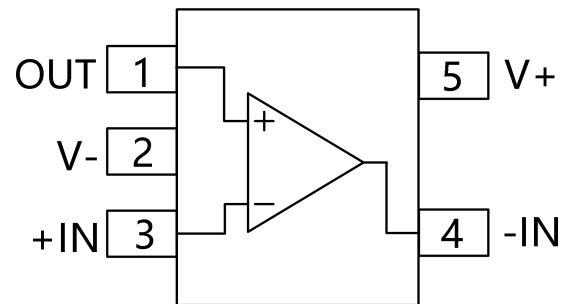
SOT23-5



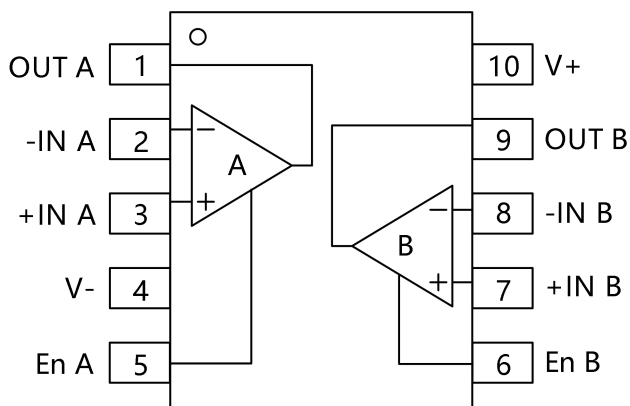
SOIC-8(SOP8), MSOP-8



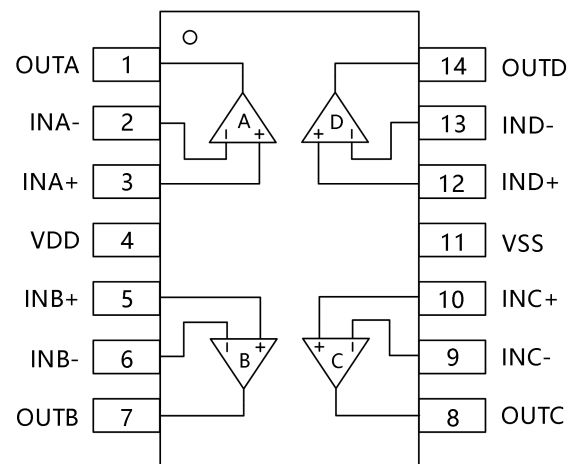
SOIC-8(SOP8), MSOP-8, TDFN2x2-8



SOT23-5



MSOP-10



SOIC-14(SOP14), TSSOP-14

Note : NC indicates no internal connection

Electrical Characteristics

- Supply Voltage, V+ to V- 7.0V
- Input Terminals, Voltage ⁽²⁾ - 0.5 to (V+) + 0.5V
 Current ⁽²⁾ ±10mA
- Storage Temperature -65°C to +150°C
- Operating Temperature -40°C to +125°C
- Junction Temperature -65°C to +150°C
- Package Thermal Resistance @ T_A = +25°C
- SOT23-5,SOT23-6 200°C/W
- MSOP-10, SOIC-8 150°C/W
- SOIC-14, TSSOP-14 100°C/W
- Lead Temperature (Soldering, 10s) 300°C
- ESD Susceptibility
- HBM 2000V
- MM 400V

1.Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

2.Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

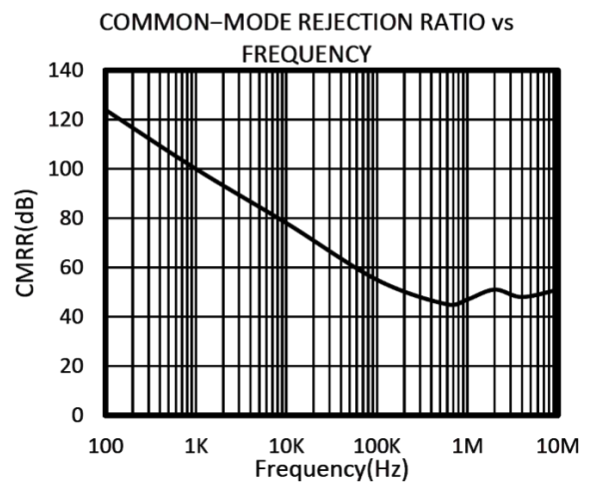
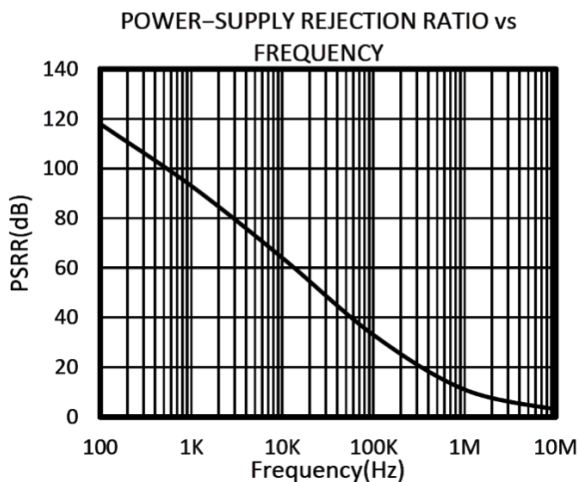
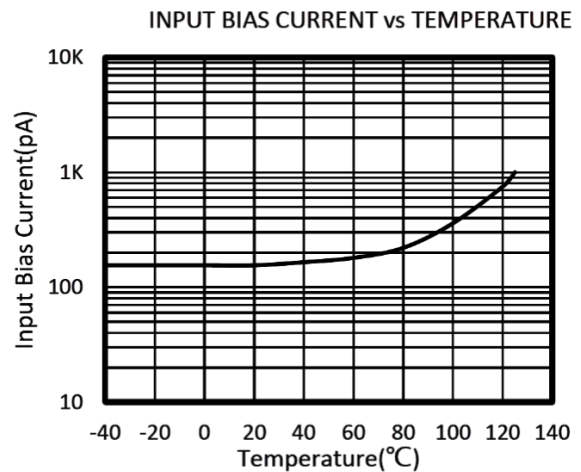
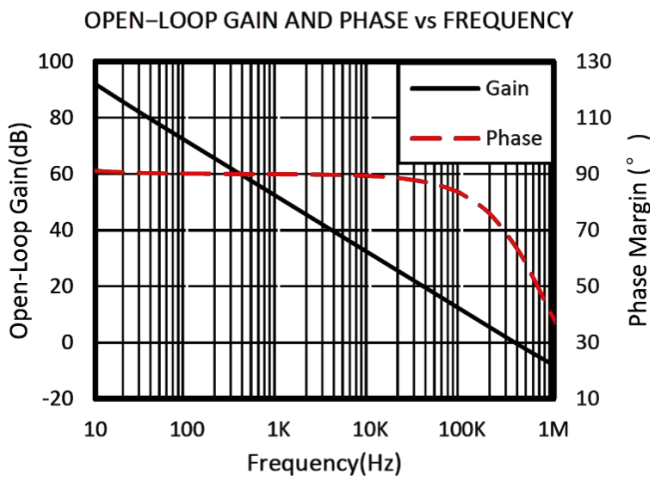
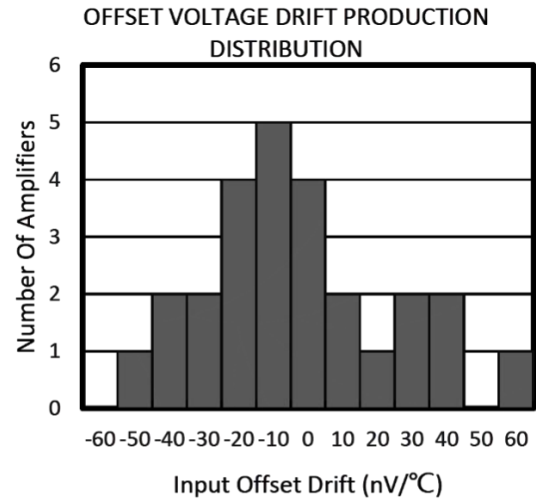
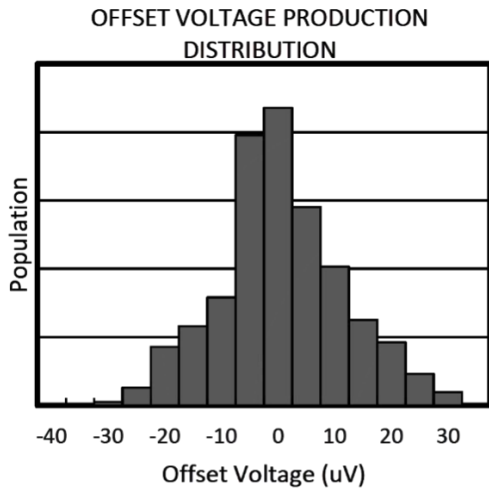
(At $T_A = +25^{\circ}\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.)

PARAMETER	CONDITION	CBM8511 ,CBM8512 CBM8513 ,CBM8514			
		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Input Offset Voltage (V_{OS})	$V_{CM} = V_S/2$		7	40	μV
VS Temperature (dV_{OS}/dT)			0.05	0.2	$\mu\text{V}/^{\circ}\text{C}$
VS Power Supply (PSRR)	$V_S = +2.5\text{V}$ to $+5.5\text{V}$, $V_{CM} = 0$	110	130		dB
Channel Separation, dc			0.1		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT					
Input Bias Current (I_B)	$V_{CM} = V_S/2$		50		pA
Input Offset Current (I_{OS})			10		pA
NOISE PERFORMANCE					
Input Voltage Noise ($e_{n,p-p}$)	$f=0.01\text{Hz}$ to 10Hz		1.6		μV_{pp}
Input Voltage Noise ($e_{n,p-p}$)	$f=0.01\text{Hz}$ to 1Hz		0.48		uV_{pp}
Input Voltage Noise Density (e_n)	$f=1\text{KHz}$		70		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise Density (i_n)	$f=10\text{Hz}$		8		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range (V_{CM})		(V-)-0.1		(V+)+0.1	V
Common-Mode Rejection Ratio (CMRR)	$(V-) - 0.1\text{V} < V_{CM} < (V+) + 0.1\text{V}$	110	130		dB
INPUT CAPACITANCE					
Differential			1		pF
Common-Mode			5		pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain (A_{OL})	$R_L=10\text{K}\Omega$, $V_O=0.3\text{V}$ to 4.7V , $-40^{\circ}\text{C}\sim 125^{\circ}\text{C}$	110	130		dB
DYNAMIC PERFORMANCE					
Slew Rate (SR)	$G=+1$		0.17		$\text{V}/\mu\text{s}$
Gain-Bandwidth Product (GBW)			350		MHz
Overload Recovery Time			6		us

OUTPUT CHARACTERISTICS					
Output Voltage High (V_{OH})	$R_L=100\text{ K}\Omega$ to GND	4.99	4.998		V
	$R_L=10\text{ K}\Omega$ to GND	4.95	4.98		V
Output Voltage Low (V_{OL})	$R_L=100\text{ K}\Omega$ to V+		1	10	mV
	$R_L=10\text{ K}\Omega$ to V+		10	30	mV
Short-Circuit Current (I_{SC})			25		mA
POWER SUOOLY					
Operating Voltage Range		2.5		5.5	V
Quiescent Current (I_Q)			60	87	mA
SHUTDOWN					
T_{OFF}			2		μs
T_{ON}			1		us
V_L (shutdown)		0		+0.8	V
V_H (amplifier is active)		0.75(V+)		V+	V
Input Bias Current of Enable Pin			50		pA
I_{QSD}			1	5	uA

Typical Characteristics

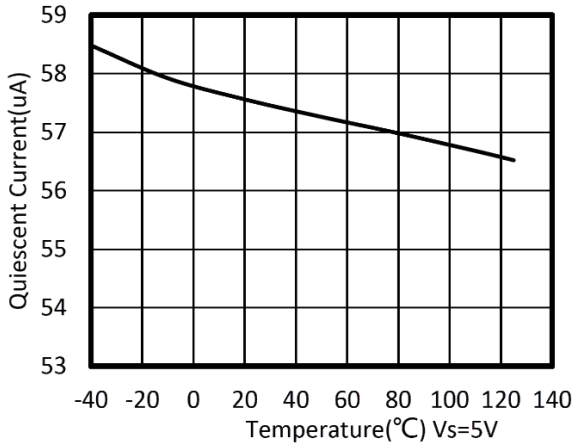
At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.



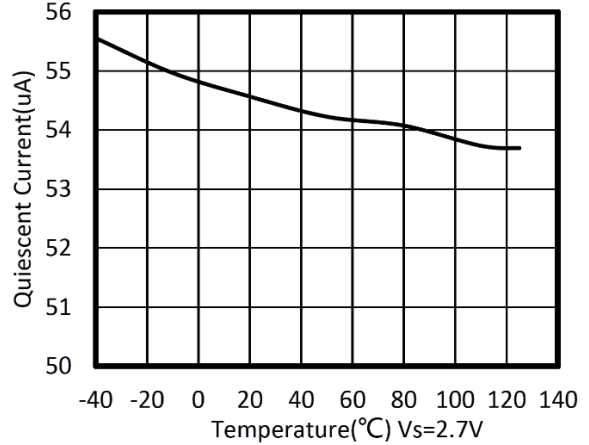
Typical Characteristics

AT $T_A = +25^\circ\text{C}$ $V_S = 5\text{V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.

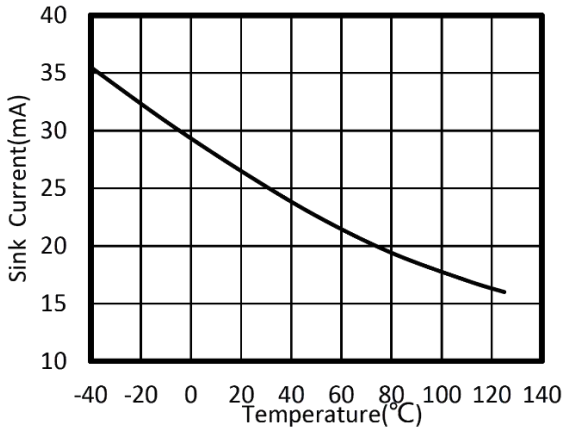
QUIESCENT CURRENT vs TEMPERATURE



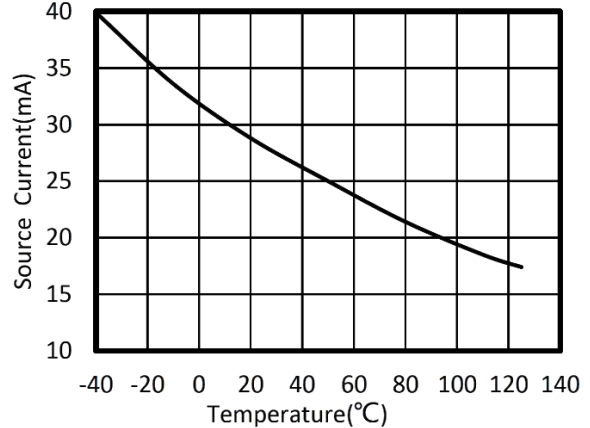
QUIESCENT CURRENT vs TEMPERATURE



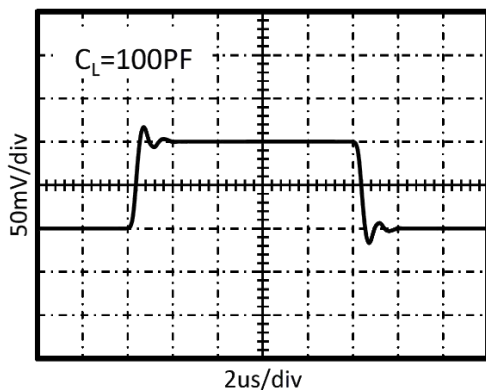
SINK CURRENT vs TEMPERATURE



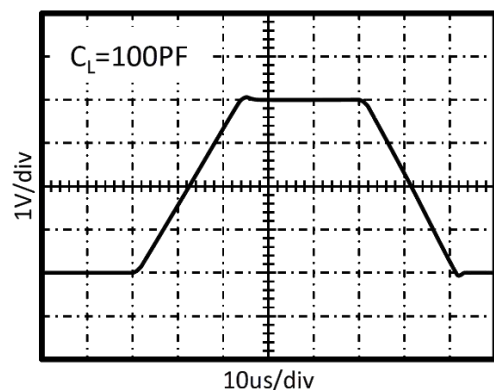
SOURCE CURRENT vs TEMPERATURE



SMALL-SIGNAL STEP RESPONSE



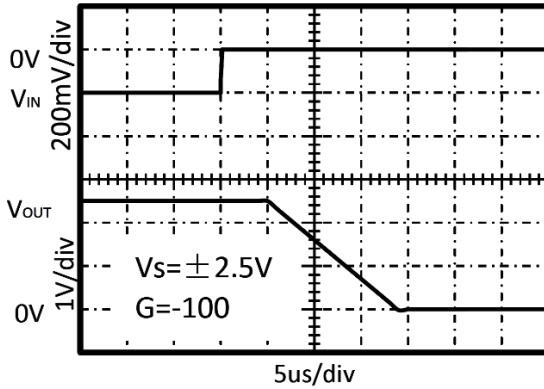
LARGE-SIGNAL STEP RESPONSE



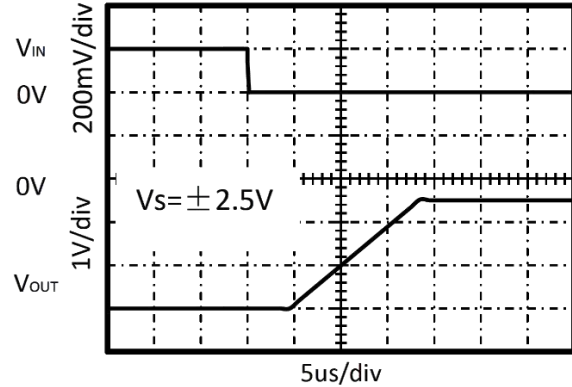
Typical Characteristics

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.

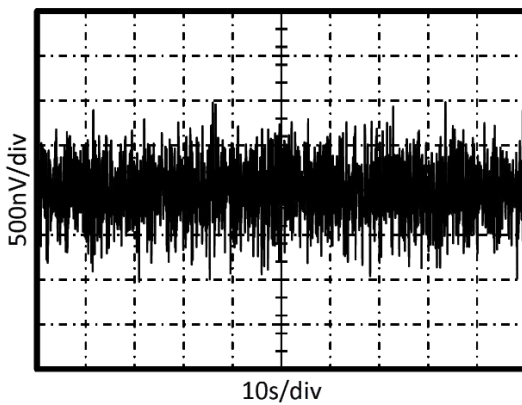
POSITIVE OVERVOLTAGE RECOVERY



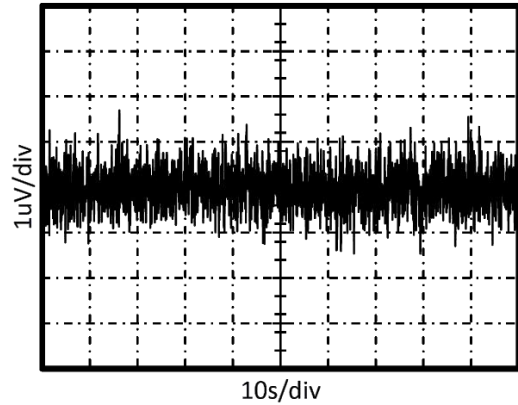
NEGATIVE OVERVOLTAGE RECOVERY



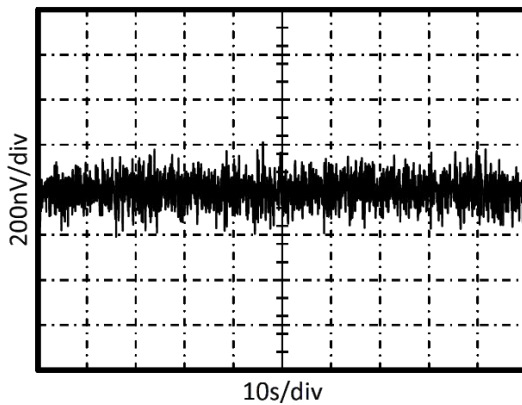
0.01Hz TO 10Hz NOISE AT $V_S = 5\text{V}$



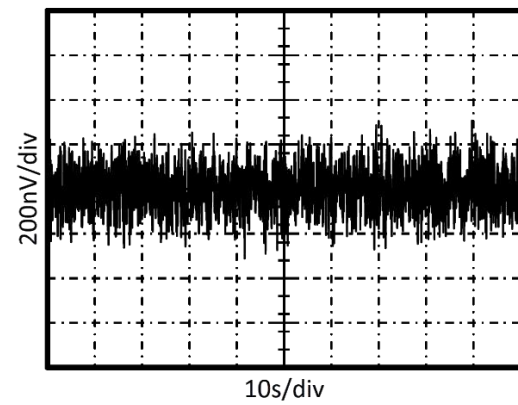
0.01Hz TO 10Hz NOISE AT $V_S = 2.7\text{V}$



0.01Hz TO 1Hz NOISE AT $V_S = 5\text{V}$



0.01Hz TO 1Hz NOISE AT $V_S = 2.7\text{V}$



Application Notes

The CBM8511, CBM8512, CBM8513, CBM8514

series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1 μ F capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

Use low thermoelectric-coefficient connections (avoid dissimilar metals).

Thermally isolate components from power supplies or other heat-sources.

Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μ V/ $^{\circ}$ C or higher, depending on materials used.

Operating Voltage

The CBM8511, CBM8512, CBM8513, CBM8514 series op amps operate over a power-supply range of +2.5V to +5.5V (\pm 1.25V to \pm 2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

CBM8513 Enable Function

The enable/shutdown digital input is referenced to the V–supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as $> 75\%$ of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as $< 0.8V$ above the V– supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time includes one full autozero cycle required by the amplifier to return to VOS accuracy. Prior to this time, the amplifier

functions properly, but with unspecified offset voltage.

Disable time is 1 μ s. When disabled, the output assumes a high-impedance state. This allows the CBM8513 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to

the device pins as possible. Place a 0.1 μ F capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility

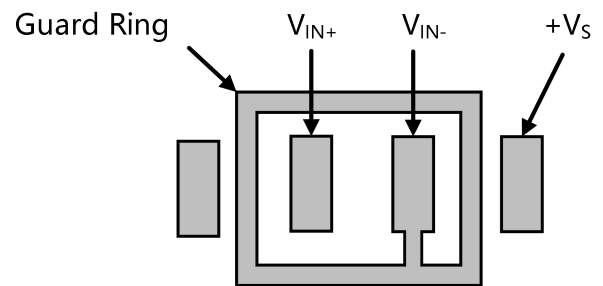
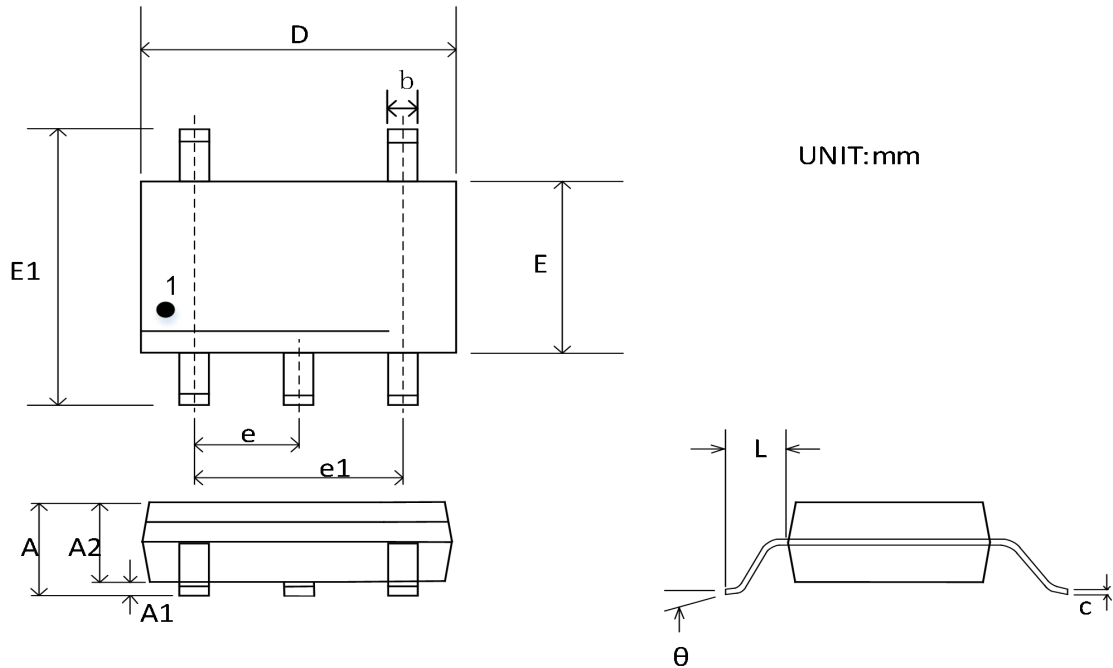


Figure 1. The Layout of Guard Ring

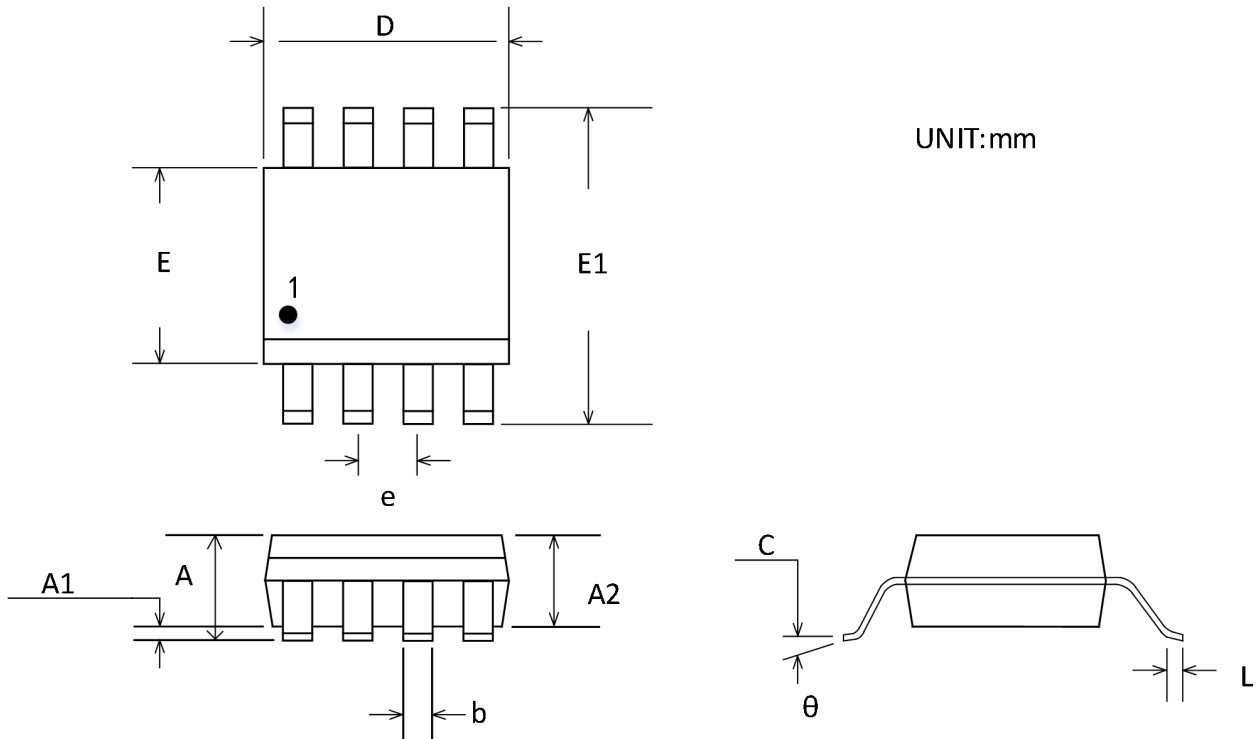
Package Outline Dimensions

SOT23-5



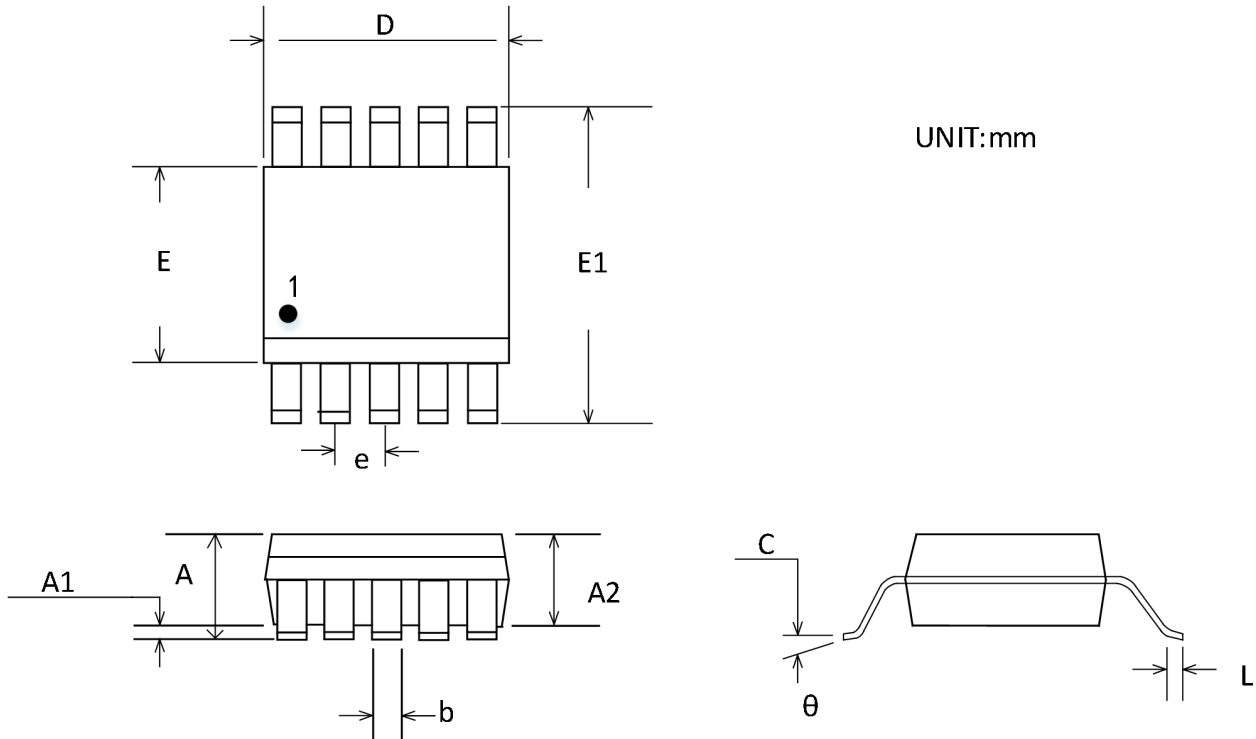
Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

MSOP-8



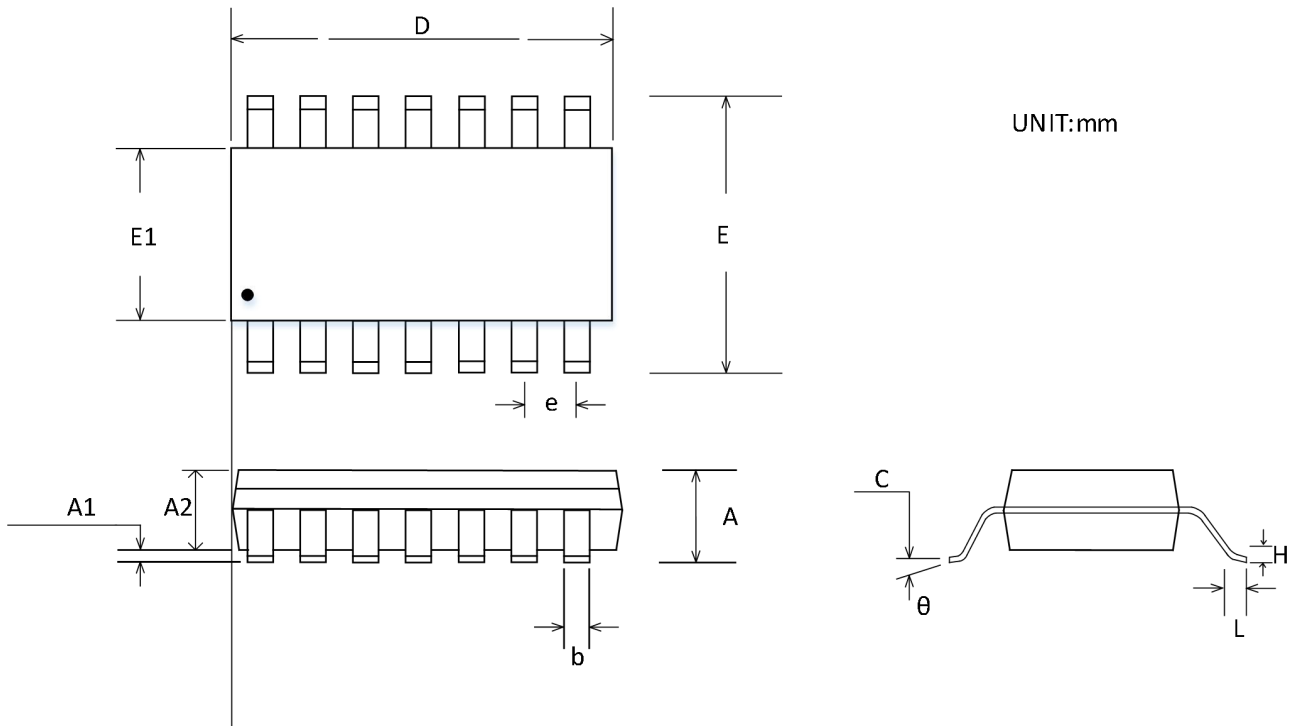
Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

MSOP-10



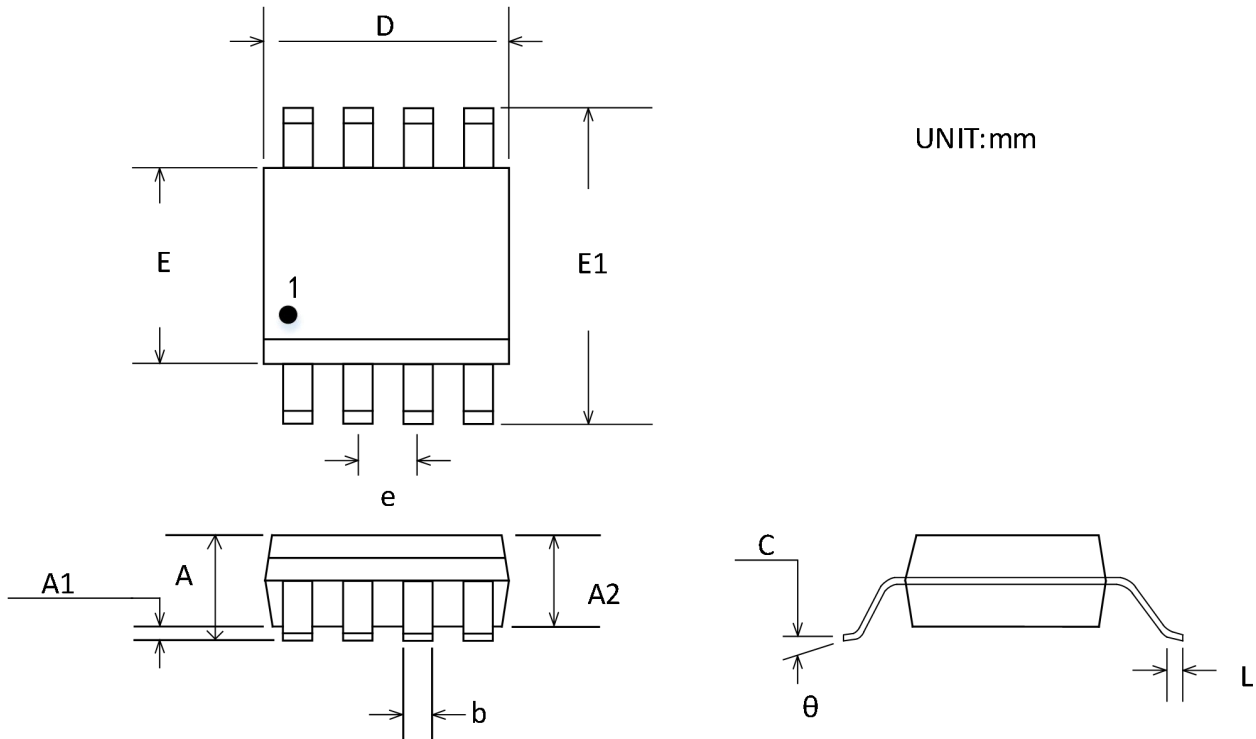
Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.50 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

TSSOP-14



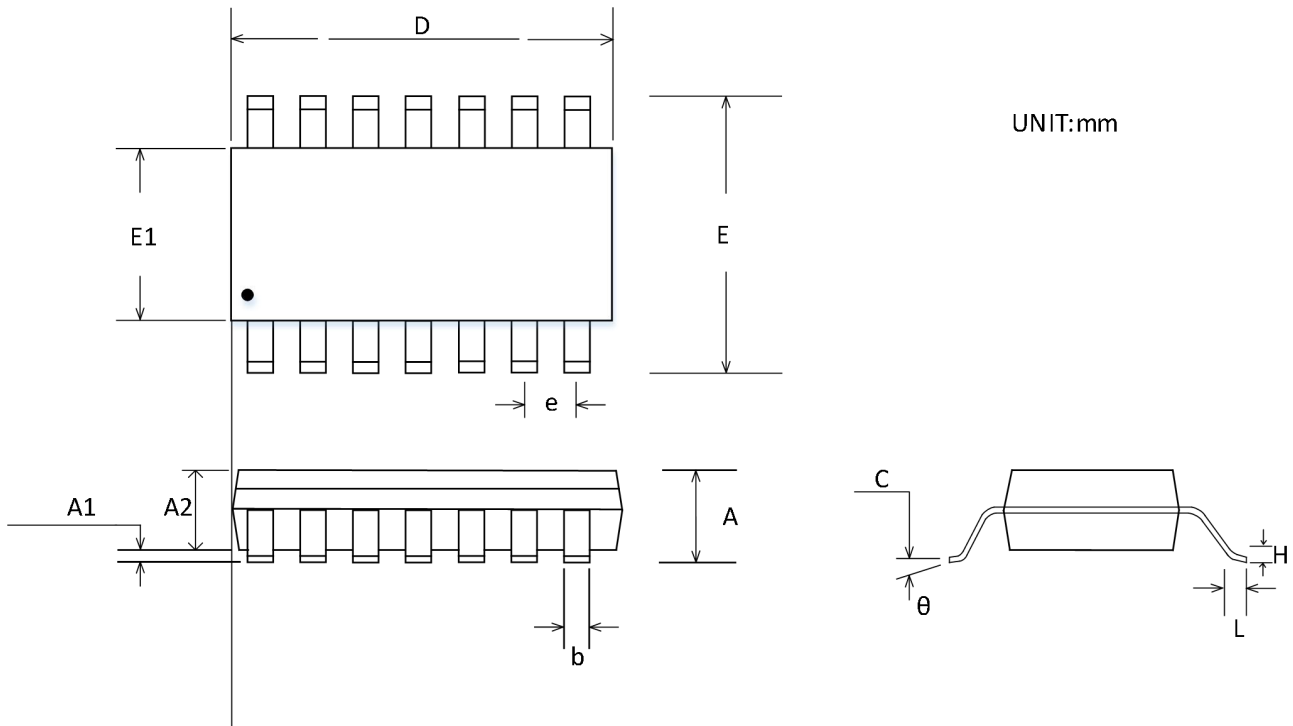
Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.020	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

SOIC-8(SOP8)



Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOIC-14(SOP14)



Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package/Ordering Information

ORDERING	TEMPRANGE	PACKAGE	PAKEAGE	TRANSPOT
CBM8511AST5	-40°C~125°C	SOT23-5	8511	Tape and Reel, 3000
CBM5811BST5	-40°C~125°C	SOT23-5	511B	Tape and Reel, 3000
CBM8511AS8	-40°C~125°C	SOIC-8(SOP8)	CBM8511A	Tape and Reel, 2500
CBM8511AS8-RL	-40°C~125°C	SOIC-8(SOP8)	CBM8511A	Tape and Reel, 3000
CBM8511AS8-REEL	-40°C~125°C	SOIC-8(SOP8)	CBM8511A	Tape and Reel, 4000
CBM8511AMS8	-40°C~125°C	MSOP-8	A11	Tape and Reel, 3000
CBM8512AS8	-40°C~125°C	SOIC-8(SOP8)	CBM8512A	Tape and Reel, 2500
CBM8512AS8-RL	-40°C~125°C	SOIC-8(SOP8)	CBM8512A	Tape and Reel, 3000
CBM8512AS8-REEL	-40°C~125°C	SOIC-8(SOP8)	CBM8512A	Tape and Reel, 4000
CBM8512AMS8	-40°C~125°C	MSOP-8	A12	Tape and Reel, 3000
CBM8512ATDE8	-40°C~125°C	TDFN-2x2-8	12AD	Tape and Reel, 3000
CBM8513AMS	-40°C~125°C	MSOP-10	M13	Tape and Reel, 3000
CBM8514AS14	-40°C~125°C	SOIC-14(SOP14)	CBM8514AS	Tape and Reel, 2500
CBM8514AS14-RL	-40°C~125°C	SOIC-14(SOP14)	CBM8514AS	Tape and Reel, 3000
CBM8514AS14-REEL	-40°C~125°C	SOIC-14(SOP14)	CBM8514AS	Tape and Reel, 4000
CBM8514ATS14	-40°C~125°C	TSSOP-14	CBM8514AT	Tape and Reel, 2500
CBM8514ATS14-RL	-40°C~125°C	TSSOP-14	CBM8514AT	Tape and Reel, 3000
CBM8514ATS14-REEL	-40°C~125°C	TSSOP-14	CBM8514AT	Tape and Reel, 4000