Application

- Communication for wireless and broad-band
- receiver
- Communication Test Equipment
- subsystem of Radar and satellite
- Power Amplifier linearization

Features

- Resolution：14bit
- sample rate：250MSPS
- SNR > 65dB；
- SFDR > 70dB；
- Power Consumption:< 0.45W
- PIN and ADS4149 series Compatible

Description

The BM41AD49QF of 14-bit A/D Converter (Analog-to-Digital Converter) with sampling rates up to 250MSPS is monolithic integrated circuits manufactured using CMOS Technology，this Converter has characteristics of high speed and high precision. A new design approach is taken advantage in this A/D Converter to achieve high dynamic performance as well as ultra-low-power at 1.8V supply. It is can be used for multi-carrier broadband communication application.

The elementary diagram of A/D Converter. This circuit include pipelining processing, out driver circuit, internal generation reference circuit, Clock duty cycle stabilizer, control logic and digital Correction circuit.

This circuits are available in a compact QFN-48 package and can alternative similar products of ADS4149 made by Texas Instrument (TI).

Pin Configurations

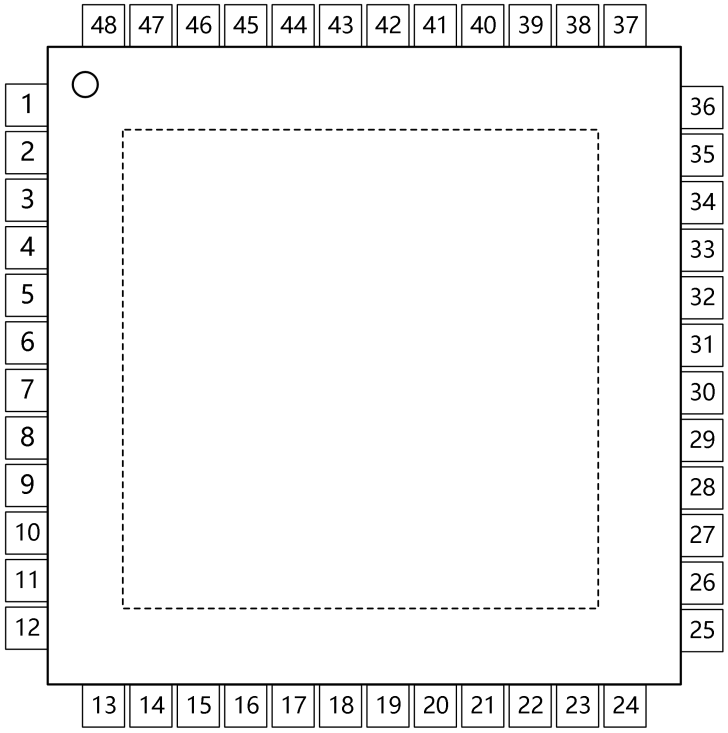


Figure 1.1. Pin Configuration

Catalog

Pin Description

Pin Number	Symbol	Pin Description	Pin Number	Symbol	Pin Description
1	GND_D	Digital ground	25	GND_A	Simulation ground
2	VDDD	Digital power	26	VDDA	Simulation power
3	QOR	Overflow bit	27	SEN	Serial interface enable
4	QCLK-	Clock output (-)	28	SDATA	Serial interface data input
5	QCLK+	Clock output (+)	29	SCLK	Serial interface clock input
6	DFS	Output data format	30	RESET	Reset
7	OE	Output enables	31	DNC	No connection
8	VDDA	Analogue power	32	DNC	No connection
9	GND_A	Analogue ground	33	DD0-/DD1-	D0、D1 Negative output of D0、D1
10	INCLK+	Differential clock input (+)	34	DD0+/DD1+	D0、D1 Positive output of D0、D1
11	INCLK-	Differential clock input (-)	35	VDDD	Digital Power
12	GND_A	Analogue ground	36	GND_D	Digital ground
13	VCM	Common-mode input	37	DD2-/DD3-	D2、D3 Negative output of D2、D3
14	GND_A	Analogue ground	38	DD2+/DD3+	D2、D3 Positive output of D2、D3
15	IN+	Differential analogue input (+)	39	DD4-/DD5-	D4、D5 Negative output of D4、D5
16	IN-	Differential analogue input (-)	40	DD5+/DD5+	D4、D5 Positive output of D4、D5
17	GND_A	Analogue ground	41	DD6-/DD7-	D6、D7 Negative output of D6、D7
18	VDDA	Analogue power	42	DD6+/DD7+	D6、D7 Positive output of D6、D7
19	GND_A	Analogue ground	43	DD8-/DD9-	D8、D9 Negative output of D8、D9
20	VDDA	Analogue power	44	DD8+/DD9+	D8、D9 Positive output of D8、D39
21	DNC	No connection	45	DD10-/DD11-	D10、D11 Negative output of

					D10、D11
22	VDDA	Analogue power	46	DD10+/DD11+	D10、D11 Positive output of D10、D11
23	DNC	Backup	47	DD12-/DD13-	D12、D13 Negative output of D12、D13
24	VDDA	Analogue power	48	DD12+/DD13+	D12、D13 Positive output of D12、D13

Figure 1.2 Pin Description

Block Diagram and Timing Characteristics

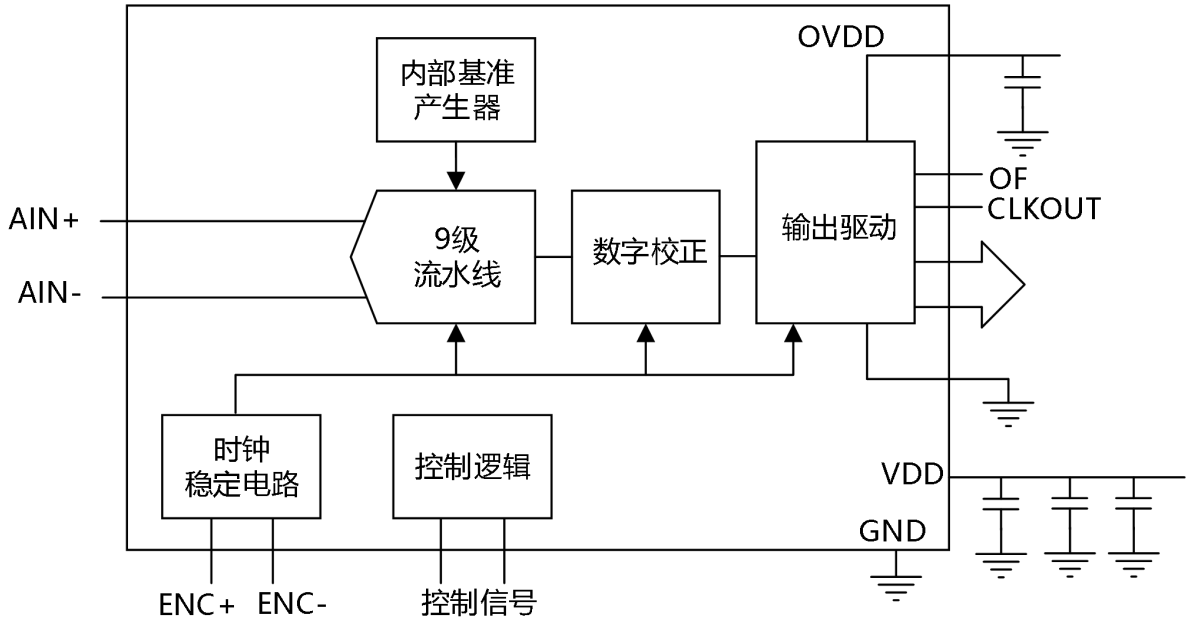


Figure 1.3 Block Diagram

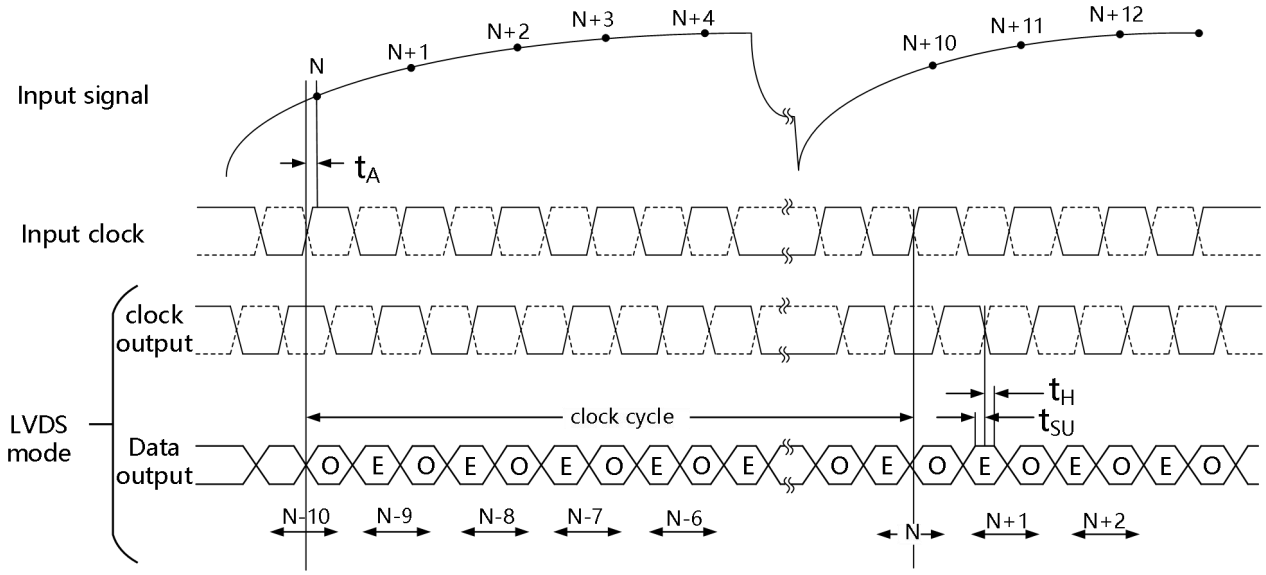


Figure 1.4 Timing characteristics

Performance Parameter

Parameter	Test Condition	14-bit 250MHz ADC			Unit
		Min	Typ	Max	
Resolution	-		14		Bit
SNR	f_{CLK}=250MHz, f_{IN}=30MHz	69	71	-	dBFS
	f_{CLK}=250MHz, f_{IN}=70MHz	68	70	-	
	f_{CLK}=250MHz, f_{IN}=170MHz	67	69	-	
SINAD	f_{CLK}=250MHz, f_{IN}=30MHz	68	70	-	dBFS
	f_{CLK}=250MHz, f_{IN}=70MHz	67	69	-	
	f_{CLK}=250MHz, f_{IN}=170MHz	66	68	-	
SFDR	f_{CLK}=250MHz, f_{IN}=30MHz	78	82	-	dBFS
	f_{CLK}=250MHz, f_{IN}=70MHz	77	80	-	
	f_{CLK}=250MHz, f_{IN}=170MHz	76	78	-	
ENOB	f_{CLK}=250MHz, f_{IN}=30MHz	10.5	-	-	Bit
DNL	f_{CLK}=250MHz, f_{IN}=10MHz	-0.99	±0.8	-	LSB
INL	f_{CLK}=250MHz, f_{IN}=10MHz	-	±3.5	±5	LSB
digital characters					
Differential Input Voltage Range	—	-	2	-	Vpp
Input Resistance	—	-	1	-	MΩ
input capacitance	—	-	4	-	pF
Analogue input bandwidth	—	-	480	-	MHz
Common-Mode Output Voltage	—	-	0.95	-	V
DC characters					
offset error	—	-15	3	15	mV
gain error	—	-2	-	2	%FS
power dissipation					
Analog Current	LVDS mode (350mV)	-	138	150	mA
digit current	LVDS mode (350mV)	-	65	80	mA
Analog power consumption	LVDS mode (350mV)	-	248.4	270	mW

Digital power consumption	LVDS mode (350mV)	-	117	144	mW
Sleep power consumption	LVDS mode (350mV)	-	3.5	25	mW
digital characters					
Input Logic Voltage High	—	1.5	-	—	V
Input Logic Voltage Low	—	—	-	0.3	V
Input Logic Voltage High	—	-15	-	15	uA
Low input current	—	-2	-	2	uA
LVDS differential output voltage	LVDS mode (350mV)	200	350	500	mV
LVDS common-mode output voltage	LVDS mode (350mV)	0.8	1.05	1.3	V
time parameter					
Aperture delay	-	0.6	0.8	1.2	ns
Data setting time	LVDS mode (350mV)	0.35	0.6	-	ns
Data holding time	LVDS mode (350mV)	0.75	1.1	-	ns

Figure 1.5 performance parameter list

Curve diagram of Main characteristics(test chart of electrical characteristics)

1、Test condition for the test result of DNL、INL:

Sampling rates (SR): f_{CLK}=250MHz;

Frequency of input signal f_{IN}=10MHz;

Test result: DNL: +0.8/-0.75 LSB

INL: +4.1/-3.8 LSB

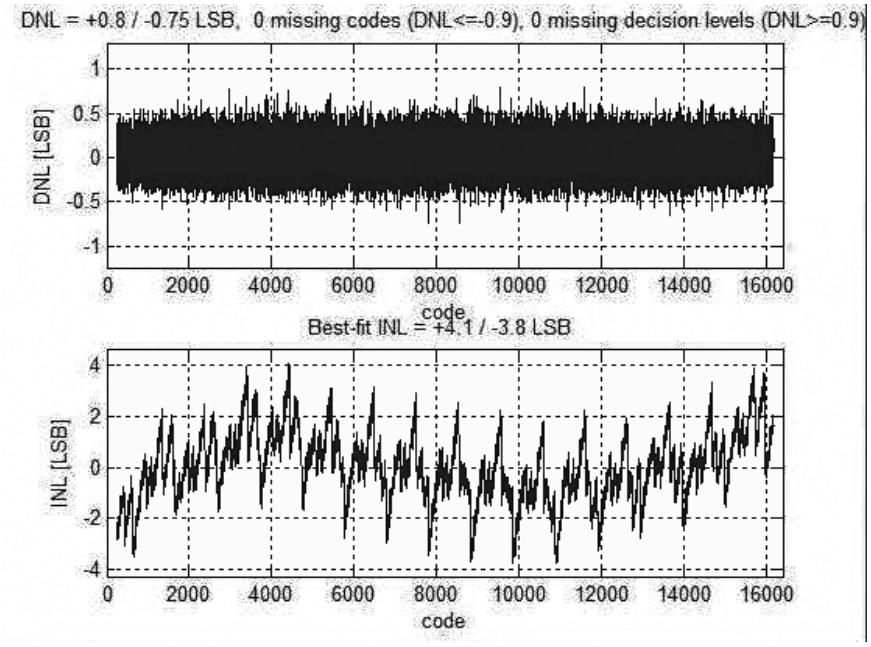


Figure 1.6 Test result of DNL and INL

2．Test condition for the test result of dynamic parameter:

Sampling rates（SR）: f_{CLK}=250MHz;

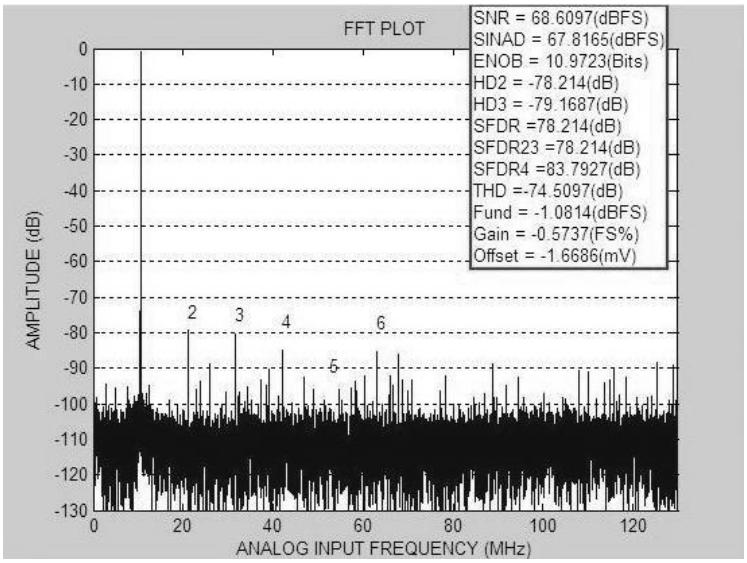
Frequency of input signal: f_{IN}=10MHz;

Test result: SFDR=78dB;

HD2，3nd=78dB;

HD4nd=83dB;

SNR=68.6dB;



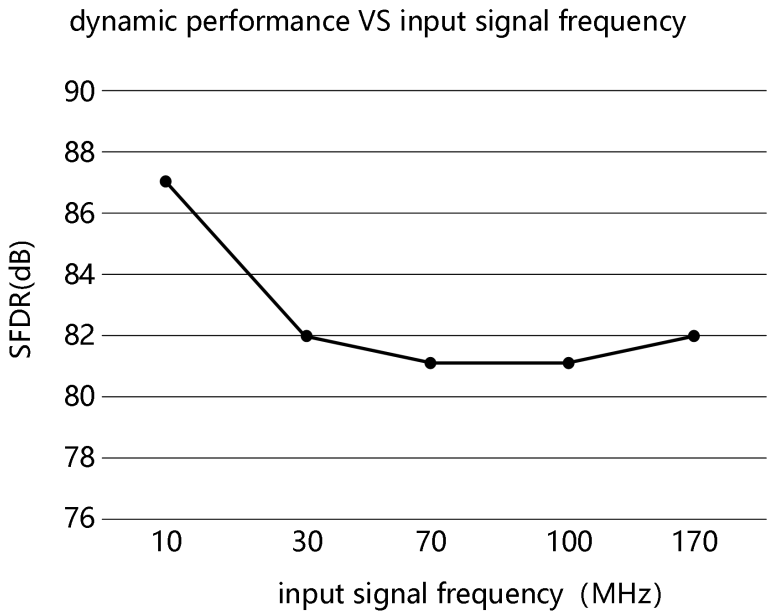


Figure 1.8 dynamic performance index VS frequency

Typical Application Circuit

1. Generation

The 14-bit A/D Converter (Analog-to-Digital Converter) is monolithic integrated circuits manufactured using CMOS Technology. It has characteristics of high sampling rate, small linear error, offset gain factor calibration, interface control and so on. Through SPI interface, the converter can configure operating condition of interior circuit, input offset and full-scale input range. The Analogue input which is differential input is AC-coupled or DC-coupled input. DC Bias is set in the interior of clock input circuit which input must be DC-coupled.

this Converter has characteristics of high speed and high precision. A new design approach is taken advantage in this A/D Converter to achieve high dynamic performance as well as ultra-low-power at 1.8V supply. It is can be used for multi-carrier broadband communication application.

2. Analogue input

Analogue input use differential structure based on open-off capacity, this structure has capacity of sampling and holding function. As shown in Figure 1.9, the differential structure appear to better AC character. The common-mode voltage of Differential input of INP and INM is 0.95V, this voltage is provided by pin $V_{CM.}$ The maximum swing of differential input is 2VPP.

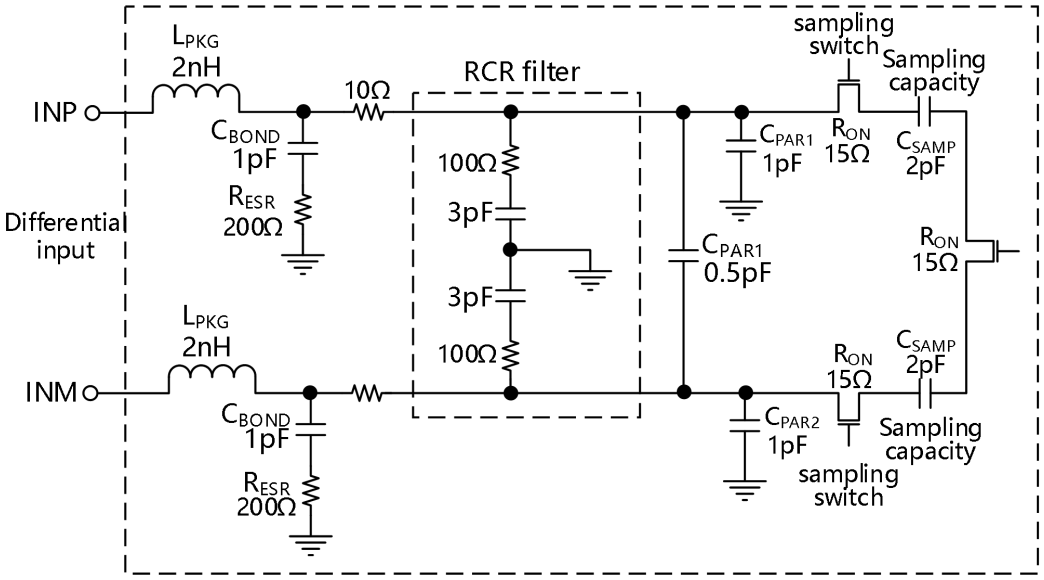


Figure 1.9 equivalent circuit of analog input

3. Driver circuit

Fig. 2.0（a）and Fig. 2.0（b）show two Configurations for driver circuit: one is optimized from low bandwidth and the other is optimized from high bandwidth (The purpose of using high bandwidth is to support high input frequency).

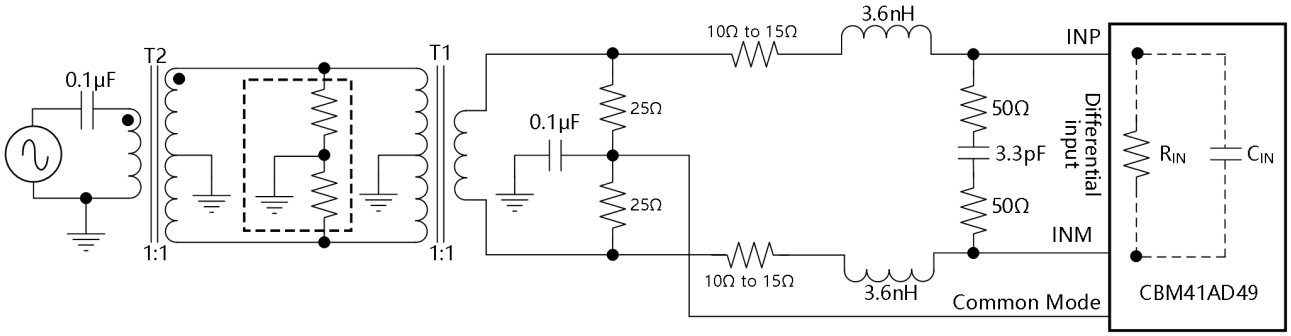


Figure 2.0（a）low-frequency analog input drive circuit

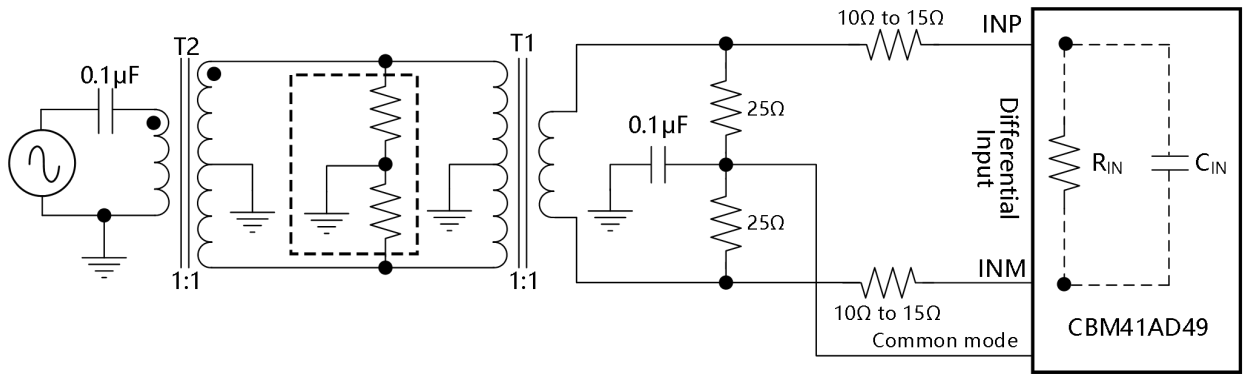


Figure 2.0 (b) high-frequency analog input drive circuit

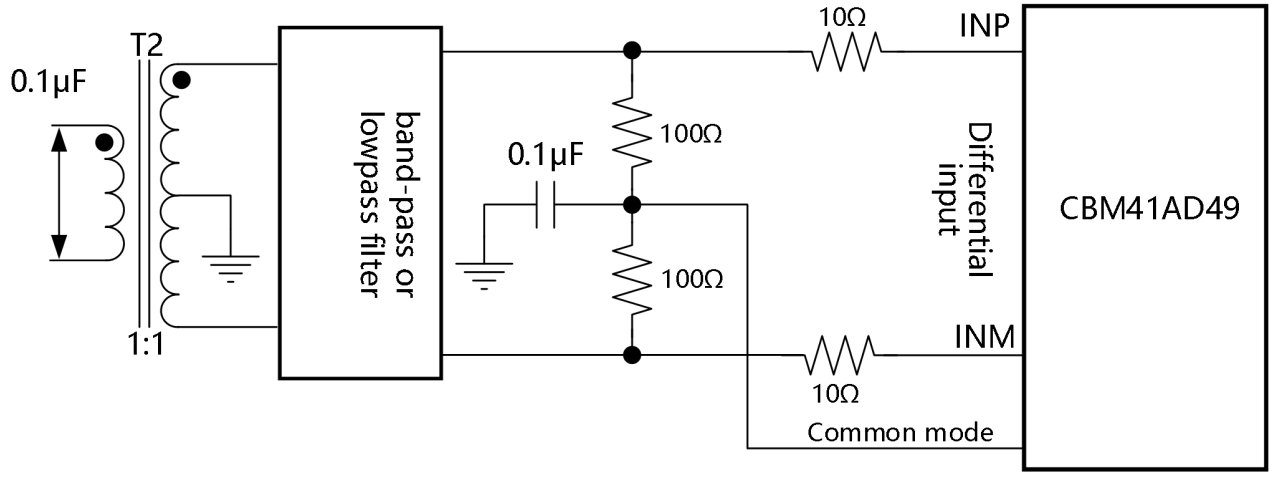


Figure 2.1 drive circuit of transformer of one forth

Figure 12 illustrates in each case aid of band pass or lowpass filters is need to obtain dynamic performance the circuit need, The result of using this filter would produce lower source impedance and the advantage of it is not only to absorption peak but also not to cause performance degradation.

4. clock input

Clock input of product can be driven by either difference (Sine wave generator, LVPECL or LVDS) or single end (LVCMOS). Application of transformer coupling in driving circuit could be adopted as sinusoidal clock signal inputting and in the same application of alternating current coupling as LVPECL or LVDS inputting. Figure 2.2 illustrates an equivalent circuit for clock input.

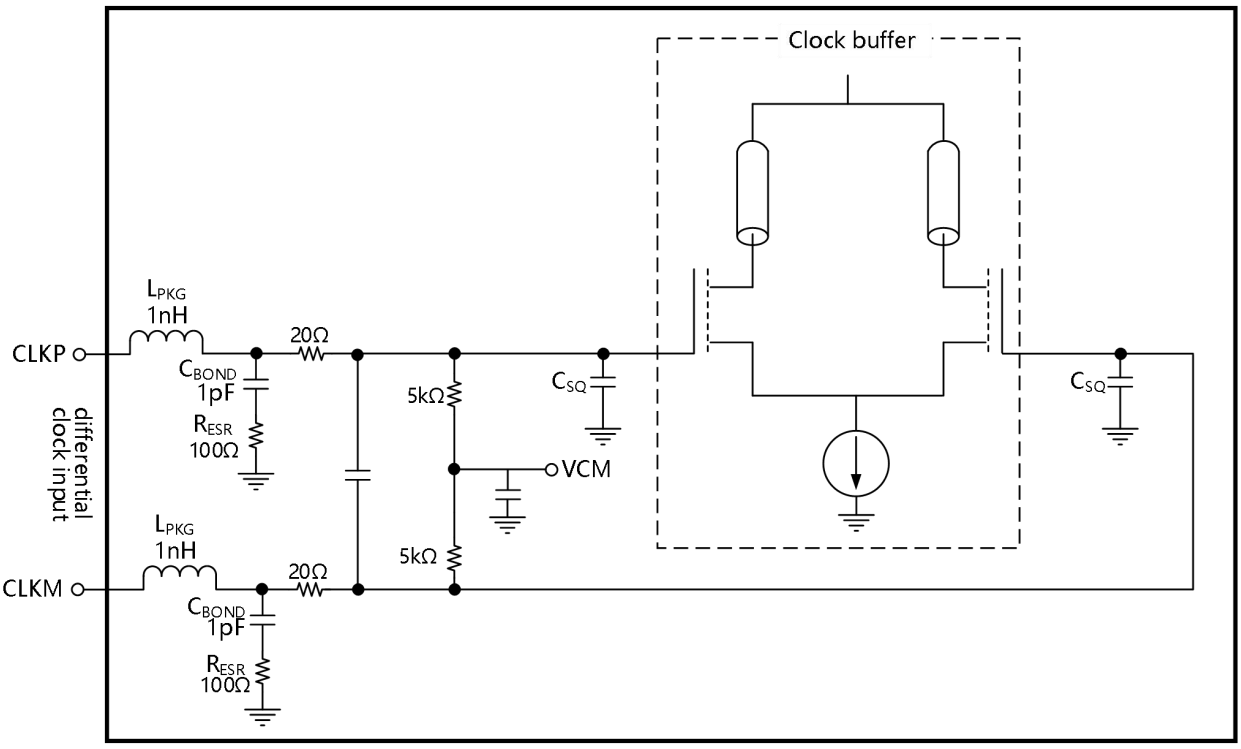


Figure 2.2 equivalent circuit of input clock

Figure 2.3 illustrates single-ended clock driving circuit , Figure 2.3 illustrates differential clock driving circuit.

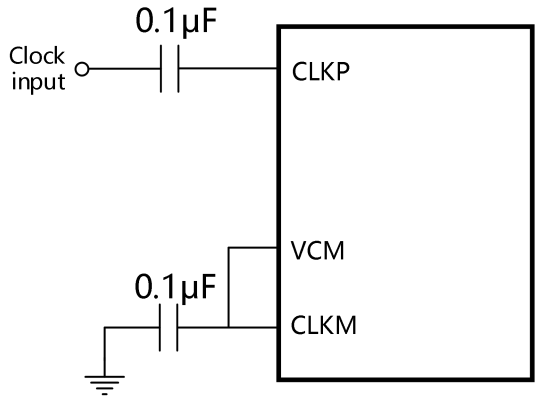


Figure 2.3 single-ended clock driving circuit

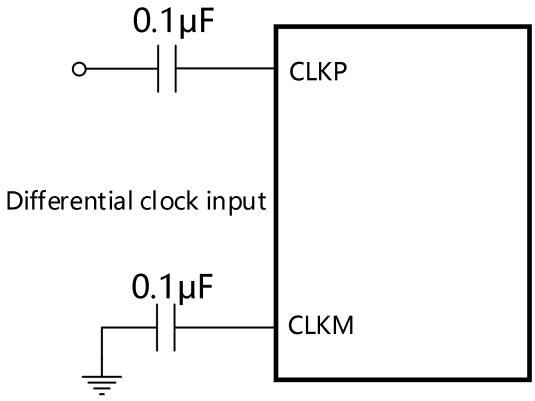


Figure 2.4 differential clock driving circuit

5. Digital Function

The default mode of devices is low latency mode and, in this mode, none digital function of devices switch ON. the 'low latency mode ' registers are filled with '1' .The function which can initialize digital function include gain calibration, Offset calibration and test mode , refer to Figure 2.5.

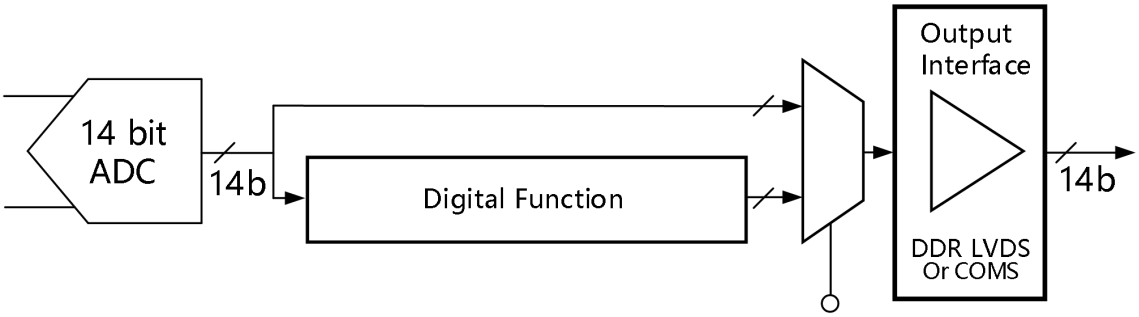


Figure 2.5 differential clock driving circuit

Matters Need Attention

1. installation:

1) The shipshape ground is required for the circuit board of application object.

2) The application object should used multiwiring board including independence ground layer.

3) The digital grounding and analog grounding of circuit board of application object should be separated as far as possible, digital line can not arrange beside of analog line or under the ADC.

4) AVDD, DRVDD and VCM should connect to ceramic bypass capacity of high quality and bypass capacity should approach pins, the line connecting pins to the bypass capacity is the shorter the better and the wider the better.

2. usage:

1) Differential input should approach as much as possible and parallel each other.

2) Input wires should be short as much as possible to minimize the input of parasitic capacitance and noise.

3) For better rejection of heat and obtain better performance, motherboard of chip should be soldering to the big ground terminal of PCB, in this way thermal performance of package would be take advantage to the maximum.

4) It is important that the ground of chip should be connected to the PCB through as many channels as possible and plentiful area.

3. protection:

1) Electrostatic Charge is easy to accumulate on human body and test equipment, discharge will be probably generated in the case of without notice. Although this product has special protection circuit for ESD, high energy electrostatic discharge may cause permanent damage to the device. It is recommended that the appropriate measure of ESD protective

should be taken to avoid that the devices not to meet its published specifications or loss function.

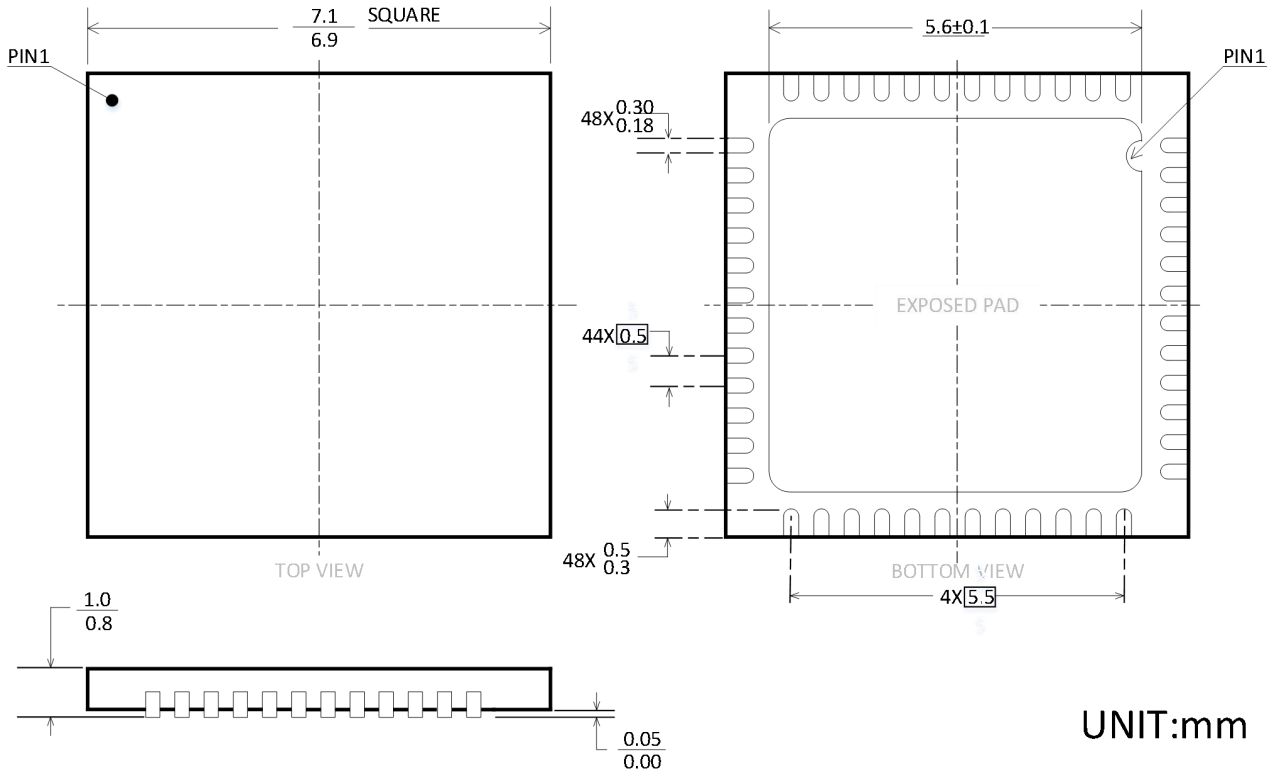
2) Stresses beyond those listed under "maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Common Failure Treatment method

1. zero output signal: Checking whether the Power supply voltage, Input Signal or clock are correct loading.
2. overflow signal occurs: Checking whether reference circuit is normal operation and whether amplitude of input signal is OK.
3. the device is unstable: Checking the power for guaranteeing stability of supply voltage

Package Outline Dimensions

QFN-48



UNIT:mm

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PAKEAGE OPTION	MAKING INFORMATION
CBM41AD49QF		-40℃-85℃	QFN-48	Tray，260	