Features

- Eight Low-Noise PGAs and Eight High-Resolution ADCs
- Input-Referred Noise: 4 μVPP (150 Hz BW, G = 6)
- Input Bias Current: 200 pA
- Data Rate: 250 SPS to 32 kSPS
- CMRR: –115 dB
- Programmable Gain: 1, 2, 3, 4, 6, 8,12 or 24
- Unipolar or Bipolar Supplies:
  – AVDD = 2.7 V to 5.5 V
  – DVDD = 1.7 V to 3.3 V
- Built-In Right Leg Drive Amplifier, Lead-Off Detection, Wilson Center Terminal, Pace Detection, Test Signals
- Integrated Respiration Impedance Measurement
- Digital Pace Detection Capabilit
- Built-In Oscillator and Reference
- SPI™-Compatible Serial Interface
- ADS1298 Pin Compatible and Program Compatible"
- Operating Temperature Range: -40°C to +85°C"

Applications

- Medical Instrumentation (ECG, EMG, and EEG)
- Patient Monitoring; Holter, Event, Stress, and Vital Signs Including ECG,
- AED, Telemedicine Bispectral Index (BIS),
- Evoked Audio Potential (EAP), Sleep Study Monitor

General Description

The CBM24AD98Q chip is a low-noise, 24-bit synchronized sampling Δ-Σ analog-to-digital converter (ADC), featuring an integrated programmable gain amplifier (PGA), internal voltage reference, and internal oscillator. The CBM24AD98Q encompasses all common functionalities required for electrocardiogram (ECG) and extracranial electroencephalogram (EEG) applications. With its high level of integration and superior performance, the CBM24AD98Q enables the creation of scalable medical instrumentation systems with significantly reduced size, power consumption, and overall cost.Each channel of the CBM24AD98Q includes a flexible input multiplexer, which can be independently connected to internally generated signals for testing, temperature measurements, and lead-off detection. Furthermore, the chip allows for flexible configuration in generating the right leg drive signal. Integrated within the chip are three amplifiers used to generate the Wilson Central Terminal (WCT) and Goldberger Central Terminal (GCT) required for standard 12-lead ECGs.The CBM24AD98Q supports both low-power and high-precision modes, with data sampling rates ranging from 250 samples per second (SPS) up to 32 kilosamples per second (kSPS). For high-channel count systems, multiple CBM24AD98Q chips can be cascaded in a daisy-chain configuration.The CBM24AD98Q is available in either a TQFP-64 package (10mm10mm) or a QFN-64 package (9mm9mm), with an operating temperature range rated from –40°C to +85°C.

Catalog

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Functional Block Diagram

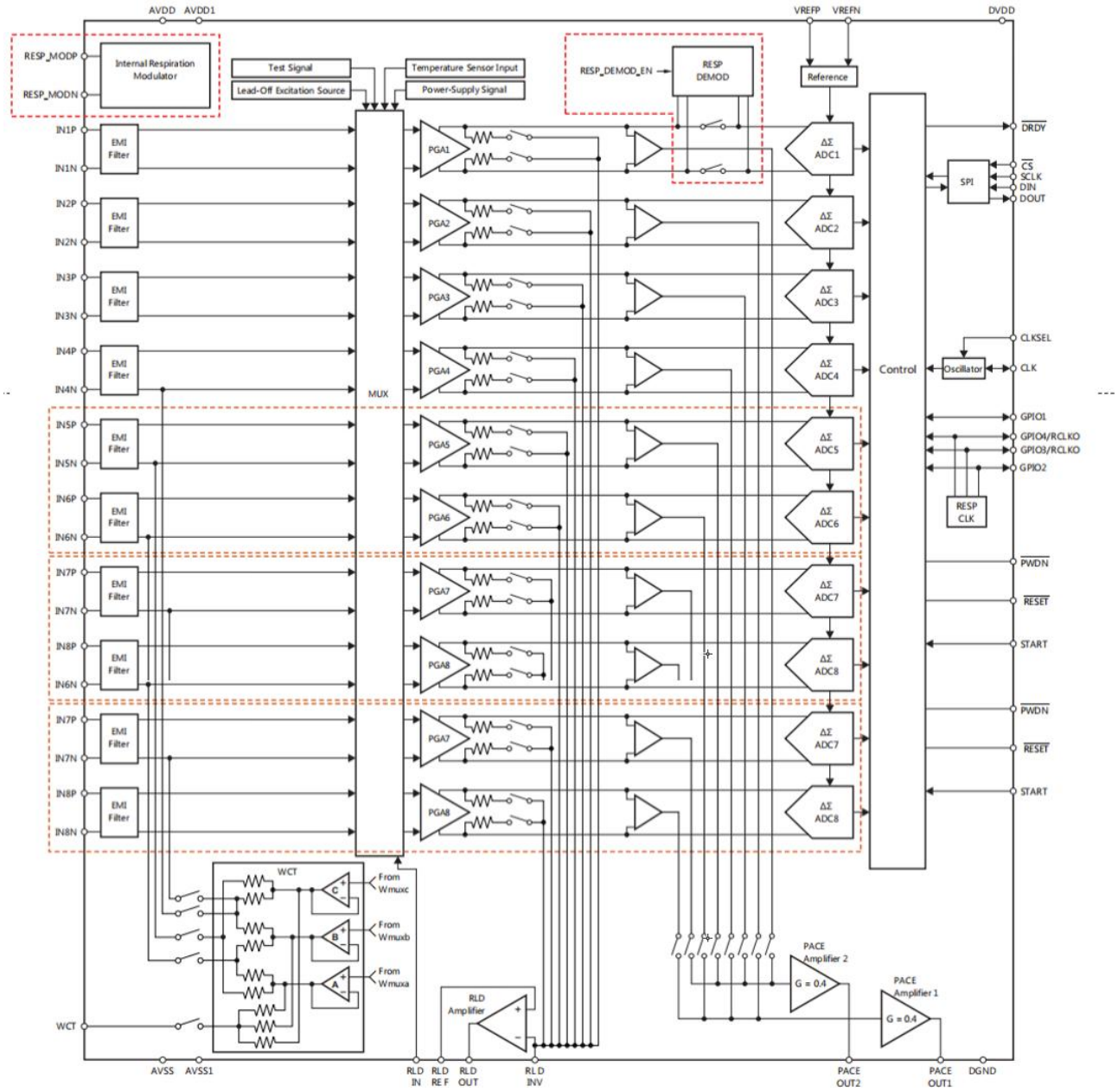
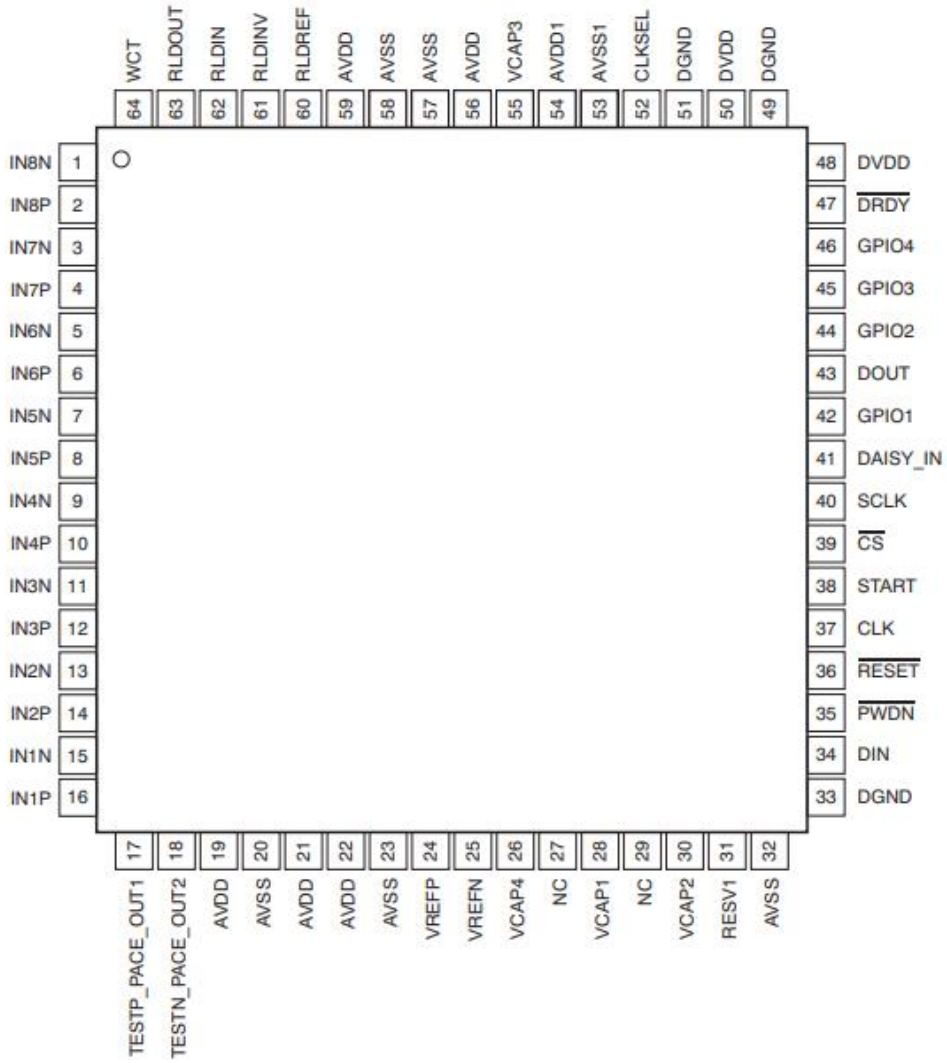


Figure 1. Functional Block Diagram

Product comparison

Model	Package	Temperature	Channel	Resolution	Maximum sampling rate
CBM24AD99Q	TQFP-64	-40℃~85℃	8	24	16kSPS
CBM24AD98Q	TQFP-64	-40℃~85℃	8	24	32kSPS

Pin configuration and functions



PIN		TYPE	DESCRIPTION
NO.	NAME		
AVDD	19,21,22,56,59	Supply	Analog supply
	59	Supply	Analog supply
AVDD1	54	Supply	Analog supply
AVSS	20,23,32,57	Supply	Analog supply
	58	Supply	Analog supply
AVSS1	53	Supply	Analog supply
BIASIN /RLDIN	62	Analog input	Right leg drive input to mux
BIASINV/ RLDINV	61	Analog input/output	Right leg drive inverting input
BIASOUT/ RLDOUT	63	Analog output	Right leg drive output
BIASREF/ RLDREF	60	Analog input	Right leg drive noninverting input
$\overline{CS}$/CS_	39	Digital input	SPI chip select; active low
CLK	37	Digital input	External Master clock input or internal clock output.
CLKSEL	52	Digital input	Master clock select
DAISY_IN	41	Supply	Daisy-chain input; if not used, short to DGND.
DGND	33,49,51	Digital input	Digital ground
DIN	34	Digital input	SPI data input
DOUT	43	Digital output	SPI data output
$\overline{DRDY}$/DR DY_	47	Digital output	Data ready; active low
DVDD	48,50	Supply	Digital power supply
GPIO1	42	Digital input/output	General-purpose input/output pin 1
GPIO2	44	Digital input/output	General-purpose input/output pin 2
GPIO3	45	Digital input/output	General-purpose input/output pin 3

GPIO4	46	Digital input/output	General-purpose input/output pin 4
IN1N	15	Analog input	Differential analog negative input 1
IN1P	16	Analog input	Differential analog positive input 1
IN2N	13	Analog input	Differential analog negative input 2
IN2P	14	Analog input	Differential analog positive input 2
IN3N	11	Analog input	Differential analog negative input
IN3P	12	Analog input	Differential analog positive input 3
IN4N	9	Analog input	Differential analog negative input 4
IN4P	10	Analog input	Differential analog positive input 4
IN5N	7	Analog input	Differential analog negative input 5(limited to CBM24AD98Q-6 and CBM24AD98Q)
IN5P	8	Analog input	Differential analog positive input 5(limited to CBM24AD98Q-6 and CBM24AD98Q)
IN6N	5	Analog input	Differential analog negative input 6(limited to CBM24AD98Q-6 and CBM24AD98Q)
IN6P	6	Analog input	Differential analog positive input 6(limited to CBM24AD98Q-6 and CBM24AD98Q)
IN7N	3	Analog input	Differential analog negative input 7(limited to CBM24AD98Q)
IN7P	4	Analog input	Differential analog positive input 7(limited to CBM24AD98Q)
IN8N	1	Analog input	Differential analog negative input 8(limited to CBM24AD98Q)
IN8P	2	Analog input	Differential analog positive input 8(limited to CBM24AD98Q)
NC	27,29	--	No connection, can be connected to AVDD or AVSS with a 10-kΩ resistor
WCT	64	Analog output	Wilson Central Terminal output
$\overline{\text{RESET}}$/RESET_	36	Digital input	System-reset pin; active low
RESV1	31	Digital input	Reserved for future use; must tie to logic low (DGND).

SCLK	40	Digital input	SPI clock
SRB1/EST P_PACE_O UT1	17	Analog input/output	Internal test signal/single-ended buffer output based on register settings
SRB2/EST P_PACE_O UT2	18	Analog input/output	Internal test signal/single-ended buffer output based on register settings
START	38	Digital input	Start conversion
$\overline{\text{PWDN}}$/P WDN_	35	Digital input	Power-down pin; active low
VCAP1	28	Analog output	Analog bypass capacitor; connect 22-µF capacitor to AVSS
VCAP2	30	Analog output	Analog bypass capacitor; connect 1-µF capacitor to AVSS
VCAP3	55	Analog output	Analog bypass capacitor; internally generated AVDD + 1.9 V; connect 1-µF capacitor to AVSS
VCAP4	26	Analog output	Analog bypass capacitor; connect 1-µF capacitor to AVSS
VREFN	25	Analog input	Negative reference voltage
VREFP	24	Analog input/output	Positive reference input/output voltage

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to AVSS	-0.3	5.5	V
DVDD to DGND	-0.3	3.9	V
AVSS to DGND	-3	0.2	V
VREFP input to AVSS	AVSS-0.3	AVDD+0.3	V
Analog input voltage	AVSS-0.3	AVDD+0.3	V
Digital input voltage	DGND-0.3	DVDD+0.3	V
Digital output voltage	DGND-0.3	DVDD+0.3	V
Input current (momentary)	--	100	mA
Input current (continuous)	--	10	mA

Junction temperature, TJ	-40	150	℃
Storage temperature, Tstg	-60	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD

			UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

Recommended Operating conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
Analog power supply (AVDD – AVSS)		2.7	3	5.25	V
Digital power supply (DVDD)		1.65	1.8	3.6	V
AVDD – DVDD		-2.1	--	3.6	V
ANALOG INPUTS					
Full-scale differential input voltage range (AINP – AINN)		±VREF / Gain			V
Common-mode input voltage		See the 9.3.3			
VOLTAGE REFERENCE INPUTS					
Differential reference voltage	3-V supply VREF = (VREFP – VREFN)	--	2.5	--	V
	5-V supply VREF = (VREFP – VREFN)	--	4	--	V
Negative input (VREFN)		--	AVSS	--	V
Positive input (VREFP)		--	AVSS + 2.5	--	V
CLOCK INPUT					
External clock input frequency	CLKSEL pin = 0	1.94	2.048	2.25	MHz

DIGITAL INPUTS					
Input Voltage		DGND	--	DVDD	V
TEMPERATURE RANGE					
Operating temperature range	Commercial grade	0	--	70	℃
	Industrial grade	-40	--	85	℃

Thermal information

THERMAL METRIC(1)		CBM24AD98Q PAG(TQFP) 64PIN	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.2	℃/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	5.8	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.6	℃/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	℃/W
ψ_{JB}	Junction-to-board characterization parameter	19.2	℃/W
$R_{\theta JC(bot)}$	Connected to the shell (bottom) thermal resistance	Not applicable	℃/W

Electrical Characteristics

Min and max specifications apply for all commercial grade (T_A = 0°C to 70°C) devices, and from TA = –40°C to +85°C for industrial-grade devices. Typical specifications at T_A = 25°C. All specifications at DVDD = 1.8 V, AVDD – AVSS = 3 V (1) , V_{REF} = 2.4 V, external f_{CLK} = 2.048 MHz, data rate = 500 SPS, HR mode(2) , and gain = 6 (unless otherwise noted).

Parameter	Test Conditions	Min	Typ.	Max	Unit
ANALOG INPUTS					
Input capacitance		--	20	--	pF
Input bias current	T_A = 25°C, input = 1.5 V	--	--	±200	pA
	T_A = 0°C to 70°C, input = 1.5 V	--	±1	--	nA
	T_A = –40°C to +85°C, input = 1.5 V	--	±1.2	--	nA
DC input impedance	No lead-off	1000		--	MΩ
	Current source lead-off detection	--	500	--	MΩ
	Pullup resistor lead-off detection	--	10	--	MΩ
PGA PERFORMANCE					
Gain settings		1,2,3,4,6,8,12			

Bandwidth		See PEA explain			
ADC PERFORMANCE					
Resolution	Data rates up to 8 kSPS, no missing codes	24	--	--	Bits
	16-kSPS data rate	19	--	--	Bits
	32-kSPS data rate	17	--	--	Bits
Data rate	f_{CLK} = 2.048 MHz, HR mode	500	--	32000	SPS
	f_{CLK} = 2.048 MHz, LP mode	250	--	16000	SPS
DC CHANNEL PERFORMANCE					
Input-referred noise	Gain = 6 (3) , 10 seconds of data	--	5	---	μV_{PP}
	Gain = 6, 256 points, 0.5 seconds of dat	--	4	7	μV_{PP}
	Gain settings ≠ 6, data rates≠ 500 SPS	See Noise Measurements section			
Integral nonlinearity(4	Full-scale with gain = 6, best fit	--	8	--	ppm
	Full-scale with gain = 6, best fit,CBM24AD98Q channel 1	--	40	--	ppm
	–20 dBFS with gain = 6, best fit,CBM24AD98Q channel 1	--	8	--	ppm
Offset error		--	±500	--	μV
Offset error drift		--	2	--	μV/℃
Gain error	Excluding voltage reference error		±0.2	±0.5	%of FS
Gain drift	Excluding voltage reference drift		5		ppm/℃
Gain match between channels			0.3		%of FS

(1) Performance is applicable for 5-V operation as well. Production testing for limits is performed at 3 V.

(2) LP mode = low-power mode.

(3) Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with input shorted (without electrode resistance) over a 10-second interval.

(4) The presence of internal demodulation circuitry on channel 1 causes degradation of INL and THD. The effect is pronounced for full-scale signals and is less for small ECG-type signals.

Parameter	Test Conditions	Min	Typ.	Max	Unit

LEAD-OFF DETECT					
Frequency	See Table 1 for settings	--	0,f_{DR}/4	--	kHz
Current	See Table 16 for settings	--	6,12,18,24	--	nA
Current accuracy		--	±20%	--	
Comparator threshold accuracy		--	±30	--	mV
EXTERNAL REFERENCE					
Input impedance		--	10	--	kΩ
INTERNAL REFERENCE					
Output voltage	Register bit CONFIG3.VREF_4V = 0,AVDD ≥ 2.7 V	--	2.4	--	V
	Register bit CONFIG3.VREF_4V = 1,AVDD ≥ 4.4 V	--	4	--	V
V_{REF} accuracy		--	± 0.2%	--	
Internal reference drift	TA = 25°C	--	35	--	ppm/℃
	Commercial grade, 0°C to 70°C	--	35	--	ppm
	Industrial grade, –40°C to 85°C	--	45	--	ppm
Start-up time		--	150	--	ms
SYSTEM MONITORS					
Analog-supply reading error		--	2%	--	
Digital-supply reading error		--	2%	--	
Device wake up	From power up to DRDY low	--	150	--	ms
	STANDBY mode	--	9	--	ms
Temperature-sensor reading,voltage	TA = 25° C	--	145	--	mV
Temperature-sensor reading,coefficient		--	490	--	μV/°C
Test-signal frequency		--	f_{CLK}/ 2^{21},	--	Hz

			f^{CLK} / 2^{20}		
Test-signal voltage		--	±1,±2	--	mV
Test-signal accuracy		--	±2%	--	
CLOCK					
Internal-oscillator clock frequency	Nominal frequency	--	2.048	--	MHz
Internal clock accuracy	TA = 25°C	--	--	±0.5%	
	0°C ≤ T_A ≤ 70°C	--	--	±2%	
	–40°C ≤ T_A ≤ 85°C, industrial grade versions only	-	--	±2.5%	
Internal-oscillator start-up time			--	20	μs
Internal-oscillator power consumption		--	120	--	μW
DIGITAL INPUT/OUTPUT (DVDD = 1.65 V to 3.6 V)					
VIH High-level inpout voltage		0.8DVDD	--	DVDD+0.1	V
VIL Low-level input voltage		-0.1	--	0.2DVDD	V
VOH High-level output voltage	I_{OH} = –500 μA	DVDD-0.4	--	--	V
VOL Low-level output voltage	I_{O}L = 500 μA	--	-	0.4	V
IIN Input current	0 V < $V_{DigitalInput}$ < DVDD	-10	--	10	μA
POWER SUPPLY (RLD, WCT, AND PACE AMPLIFIERS TURNED OFF) H					
I_{AVDD} AVDD current	AVDD – AVSS = 3 V,HR mode	--	2.75	--	mA
	AVDD – AVSS = 3 V,LP mode	--	1.8	--	mA
	AVDD – AVSS = 5 V,HR mode	--	3.1	-	mA
	AVDD – AVSS = 5 V,LP mode	--	2.1	--	mA
I_{DVDD} DVDD current	DVDD = 1.8V,HR mode	--	0.3	--	mA
	DVDD = 1.8V,LP mode	--	0.3	--	mA
	DVDD = 3V,HR mode	--	0.5	--	mA

	DVDD = 3V,LP mode		--	0.5	--	mA
Power dissipation	CBM24AD98Q、AVDD–AVSS = 3V	HR mode	--	8.8	9.5	mW
		LP mode(250SPS)	--	6.0	7.0	mW
	CBM24AD98Q-6、AVDD–AVSS = 3V	HR mode	--	7.2	7.9	mW
		LP mode(250SPS)	--	5.3	6.6	mW
	CBM24AD98Q-4、AVDD–AVSS = 3V	HR mode	--	5.4	6	mW
		LP mode(250SPS)	--	4.1	4.4	mW
	CBM24AD98Q、AVDD–AVSS = 5V	HR mode	--	17.5	--	mW
		LP mode(250SPS)	--	12.5	--	mW
	CBM24AD98Q-6、AVDD–AVSS = 5V	HR mode	--	14.1	--	mW
		LP mode(250SPS)	--	10	--	mW
	CBM24AD98Q-4、AVDD–AVSS = 5V	HR mode	--	10.1	--	mW
		LP mode(250SPS)	--	8.3	--	mW
Power-down	AVDD – AVSS = 3 V		--	10	--	μW
	AVDD – AVSS = 5 V		--	20	--	μW
Standby mode	AVDD – AVSS = 3 V		--	2	--	mW
	AVDD – AVSS = 5 V		--	4	--	mW
Quiescent channel power	AVDD – AVSS = 3 V, PGA + ADC		--	818	--	μW
	AVDD – AVSS = 5 V, PGA + ADC		--	1.5	--	mW

Timing requirement: SPI serial interface

Specifications apply from TA = –40°C to +85°C (unless otherwise noted); load on DOUT = 20 pF || 100 kΩ

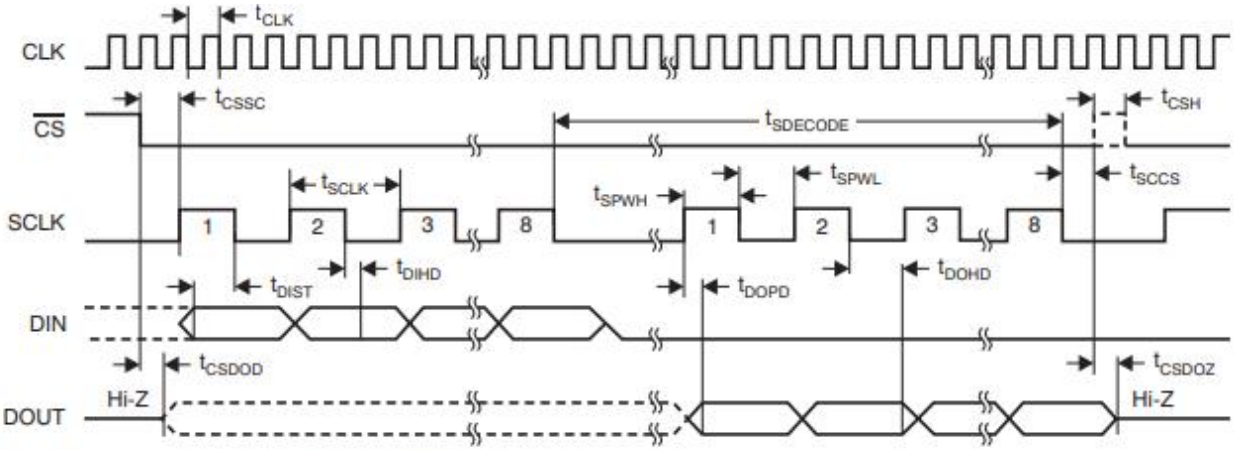
	2.7 V ≤ DVDD ≤ 3.6 V		1.65 V ≤ DVDD ≤ 2 V		UNIT
	MIN	MAX	MIN	MAX	
t_{CLK} Master clock period	414	514	414	514	ns
t_{CSSC} CS low to first SCLK, setup time	6	--	17	--	ns
t_{SCLK} SCLK period	50	--	66.6	--	ns
$S_{PWH, L}$ SCLK pulse width, high and low	15	--	25	--	ns
t_{DIST} DIN valid to SCLK falling edge: setup time	10	--	10	--	ns

t_{DIHD} Valid DIN after SCLK falling edge: hold time	10	--	11	--	ns
t_{CSH} CS high pulse	2	--	2	--	t_{CLK}
t_{SCCS} Eighth SCLK falling edge to CS high	4	--	4	--	t_{CLK}
$t_{SDECODE}$ Command decode time	4	--	4	--	t_{CLK}
$t_{DISCK2ST}$ DAISY_IN valid to SCLK rising edge: setup time	10	--	10	--	ns
$t_{DISCK2HT}$ DAISY_IN valid after SCLK rising edge: hold time	10	--	10	--	ns

Switch characteristics: SPI serial interface

Specifications apply from T_A = –40°C to +85°C (unless otherwise noted). Load on DOUT = 20 pF || 100 kΩ.

PARAMETER	2.7 V ≤ DVDD ≤ 3.6 V		1.65 V ≤ DVDD ≤ 2 V		UNIT
	MIN	MAX	MIN	MAX	
t_{DOHD} SCLK falling edge to invalid DOUT: hold time	10	--	10	--	ns
t_{DOPD} SCLK rising edge to DOUT valid: setup time	--	17	--	32	ns
t_{CSDOD} CS low to DOUT driven	10	--	20	--	ns
t_{CSDOZ} CS high to DOUT Hi-Z	--	10	--	20	ns



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 7.1. Serial Interface Timing

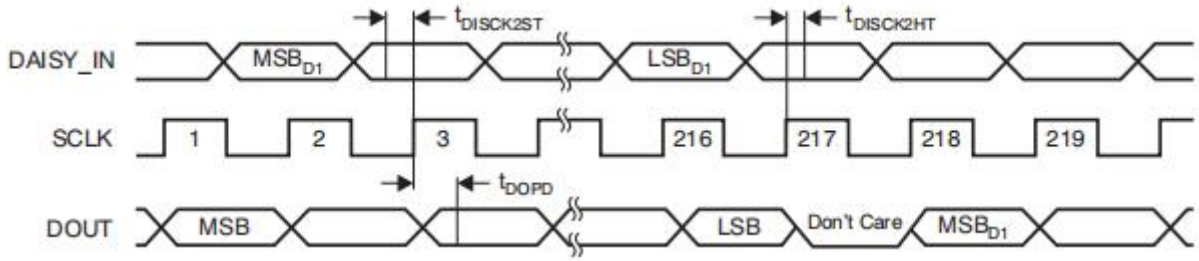


Figure 7.2. Daisy-Chain Interface Timing

Parameter measurement information

Noise measurement

Optimizing the noise performance of the CBM24AD98Q channel can be achieved by adjusting the data rate and PGA gain. Both reducing the data rate and increasing the PGA gain lead to a reduction in input noise, which is particularly beneficial for measuring weak bioelectric potential signals. The following table presents the noise performance measurements of the CBM24AD98Q under conditions of a 5V analog supply and a 4.5V reference voltage. These figures represent the typical noise performance at a temperature (TA) of +25°C. The displayed data are the averaged readings from multiple chips and were taken with the input shorted. A minimum of 1,000 consecutive readings were used to compute the RMS (μVRMS) and peak-to-peak (μVPP) noise for each measurement. For lower data rates, the ratio between RMS and peak-to-peak noise is approximately 6.6.

Table 8.1. Input-Referred Noise μV_{RMS} (μV_{PP}) in High-Resolution Mode 3-V Analog Supply and 2.4-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12
000	32000	8398	335 (3553)	168 (1701)	112 (1100)	85 (823)	58 (529)	42.5 (378)	28.6 (248)
001	16000	4193	56 (613)	28 (295)	18.8 (188)	14.3 (143)	9.7 (94)	7.4 (69)	5.2 (44.3)
010	8000	2096	12.4 (111)	6.5 (54)	4.5 (37.9)	3.5 (29.7)	2.6 (21.7)	2.2 (17.8)	1.8 (13.8)
011	4000	1048	6.1 (44.8)	3.2 (23.3)	2.4 (17.1)	1.9 (14)	1.5 (11.1)	1.3 (9.7)	1.2 (8.5)
100	2000	524	4.1 (27.8)	2.2 (15.4)	1.6 (11)	1.3 (9.1)	1.1 (7.3)	1 (6.5)	0.9 (6)
101	1000	262	2.9 (19)	1.6 (10.1)	1.2 (7.5)	1 (6.2)	0.8 (5)	0.7 (4.6)	0.6 (4.1)
110	500	131	2.1 (12.5)	1.1 (6.8)	0.9 (5.1)	0.7 (4.3)	0.6 (3.5)	0.5 (3.1)	0.5 (2.9)

Table 8.2. Input-Referred Noise μV_{RMS} (μV_{PP}) in Low-Power Mode 3-V Analog Supply and 2.4-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12
000	16000	4193	333 (3481)	166 (1836)	111 (1168)	84 (834)	56 (576)	42 (450)	28 (284)
001	8000	2096	56 (554)	28 (272)	19 (177)	14.3 (133)	9.7 (85)	7.4 (64)	5 (42.4)
010	4000	1048	12.5 (99)	6.5 (51)	4.5 (35)	3.4 (25.9)	2.4 (18.8)	2 (14.5)	1.5 (11.3)
011	2000	524	6.1 (41.8)	3.2 (22.2)	2.3 (15.9)	1.8 (12.1)	1.4 (9.3)	1.2 (7.8)	1 (6.7)
100	1000	262	4.1 (26.3)	2.2 (14.6)	1.6 (9.9)	1.3 (8.1)	1 (6.2)	0.8 (5.4)	0.7 (4.7)
101	500	131	3 (17.9)	1.6 (9.8)	1.1 (6.8)	0.9 (5.7)	0.7 (4.2)	0.6 (3.6)	0.5 (3.4)
110	250	65	2.1 (11.9)	1.1 (6.3)	0.8 (4.6)	0.7 (4)	0.5 (3)	0.5 (2.6)	0.4 (2.4)

Detailed Description

The CBM24AD98Q is a low-noise, low-power, multi-channel, simultaneous sampling, 24-bit ΔΣ analog-to-digital converter (ADC) chip, integrating a programmable gain amplifier (PGA) and various EEG-specific functionalities, making it highly suitable for applications such as electrocardiogram (ECG) and electroencephalogram (EEG). By powering down the EEG-specific circuits, these chips can also be utilized in high-performance, multi-channel data acquisition systems.This series of chips boasts a highly configurable multiplexer that facilitates temperature, power supply, input short, and bias measurements. Additionally, the multiplexer enables any input electrode to be programmed as a reference driver. The PGA gain can be selected from seven settings: 1, 2, 4, 6, 8, 12, and 24.The ADC within the chip supports data rates ranging from 250 samples per second (SPS) up to 16 kilosamples per second (kSPS). Communication with the chip is facilitated through an SPI-compatible interface and is complemented by four general-purpose input/output (GPIO) pins. Synchronization of multiple chips can be achieved using the START pin.Internally, a reference generator produces a low-noise 4.5V voltage, while an oscillator generates a 2.048 MHz clock. A versatile patient bias drive module permits the selection of any electrode combination's average to generate the patient-driven signal. Lead-off detection is accomplished via a current source.

Function Description

This section describes the internal functional information of the CBM24AD98Q. Here, f_{CLK} represents the frequency of the signal on the CLK pin, t_{CLK} denotes the period of the signal on the CLK pin, f_{DR} indicates the output data rate, t_{DR} signifies the output data time cycle, and f_{MOD} refers to the frequency at which the modulator samples the input.

Input Multiplexer

In the CBM24AD98Q, each channel is equipped with an input multiplexer (depicted in Figure 9.3.1), offering flexible signal routing options through configuration. In the diagram, MAIN signifies the conditions where MUX[2:0] is set to 000, 110, or 111.

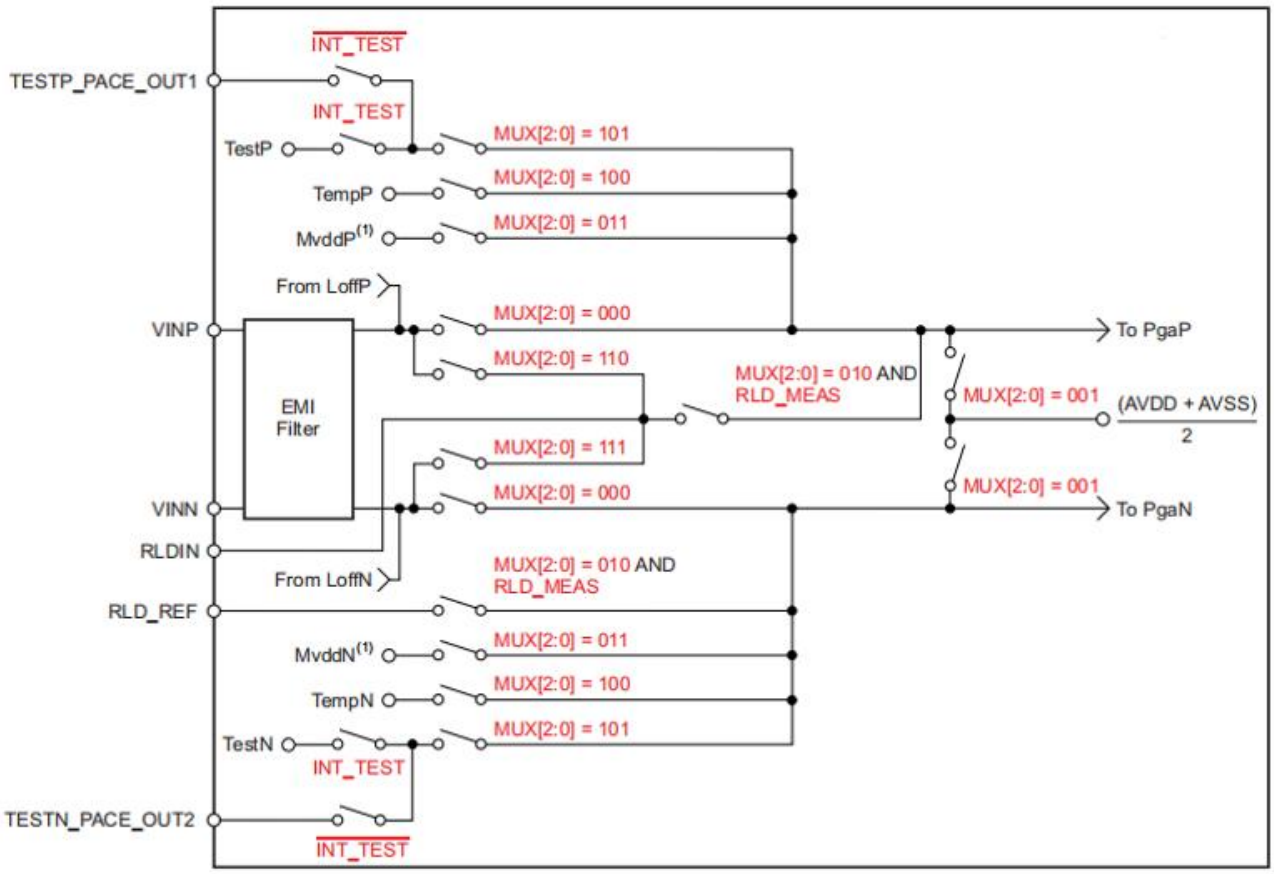


Figure 9.3.1 Multiplexer on Channel

(1) Chip Noise Measurement Setting CHnSET[2:0] to 001 shorts the P/N terminals of the channel and sets a common-mode voltage of [(VVREFP + VVREFN)/2] for both channel inputs. This configuration can be utilized for testing the inherent noise of the chip.

(2) Test Signal (TestP and TestN) Configuring CHnSET[2:0] to 101 introduces an internally generated test signal to the P/N terminals of the channel. Details regarding the internal test signal can be found in the CONFIG2 register description.

(3) Temperature Sensor (TempP, TempN) The CBM24AD98Q incorporates an on-chip temperature sensor, which employs two internal diodes, with one diode having a current density sixteen times that of the other, as depicted in Figure 9.3.2. The disparity in diode current densities generates a voltage difference proportional to the absolute temperature. Owing to the low thermal resistance from the package to the printed circuit board (PCB), the internal chip temperature is closely correlated with the PCB temperature. Note that self-heating of the CBM24AD98Q can lead to internal temperature readings higher than the ambient temperature of the surrounding PCB. Setting CHnSET[2:0] to 100 routes the temperature sensor signals to the P/N terminals of the channel.

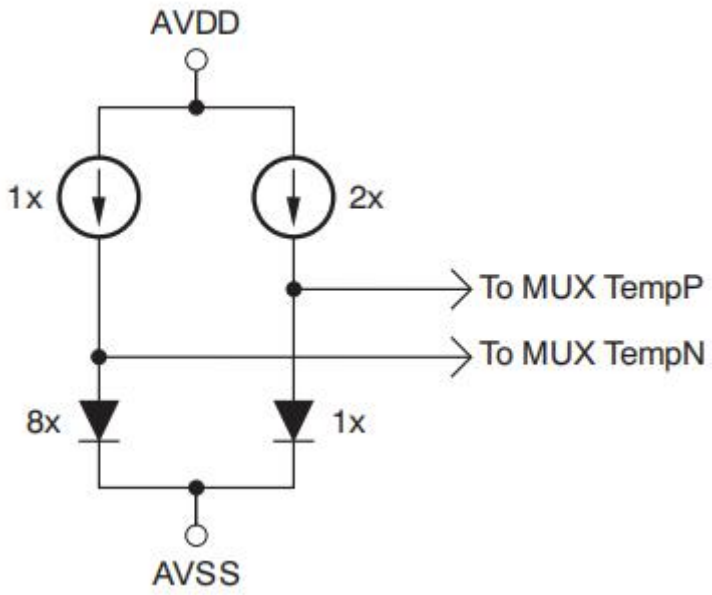


Figure 9.3.2 Illustration of Temperature Sensor Measurement Inputs

(4)Power Supply Measurement (MVDDP, MVDDN) Setting CHn SET[2:0] to 011 configures the channel inputs to monitor different supply voltages of the chip. For channels 1, 2, 5, 6, 7, and 8, (MVDDP – MVDDN) equals [0.5 × (AVDD + AVSS)]. For channels 3 and 4, (MVDDP – MVDDN) is DVDD / 4. To prevent PGA saturation during power supply measurement, set the gain to 1.

(5) Lead-Off Excitation Signals (LoffP, LoffN) Lead-off excitation signals are fed into the multiplexer before switching. The comparators detecting lead-off conditions are also connected to the multiplexer prior to switching. For detailed explanation, refer to the Lead-off Detection section. (6) Single-Ended Input Measurement Mode Setting CHnSET[2:0] to 011 or 111 routes the bias signal from the BIASIN pin to the designated electrode, enabling the channel to operate as a single-ended input channel. Setting CHnSET[2:0] to 010 and setting the BIAS_MEAS bit in the CONFIG3 register to "1" measures the signal on the BIASIN pin relative to the voltage on the BIASREF pin.

9.3.2 Analog Inputs The analog inputs of the chip are connected to a low-noise, low-drift, high-input impedance programmable gain amplifier via a multiplexer. The CBM24AD98Q analog inputs are fully differential. The range of the differential input voltage (VINxP – VINxN) spans from –VREF/Gain to VREF/Gain. There are two methods to drive the analog inputs of the CBM24AD98Q: pseudo-differential or fully differential, as illustrated in Figure 9.3.3.

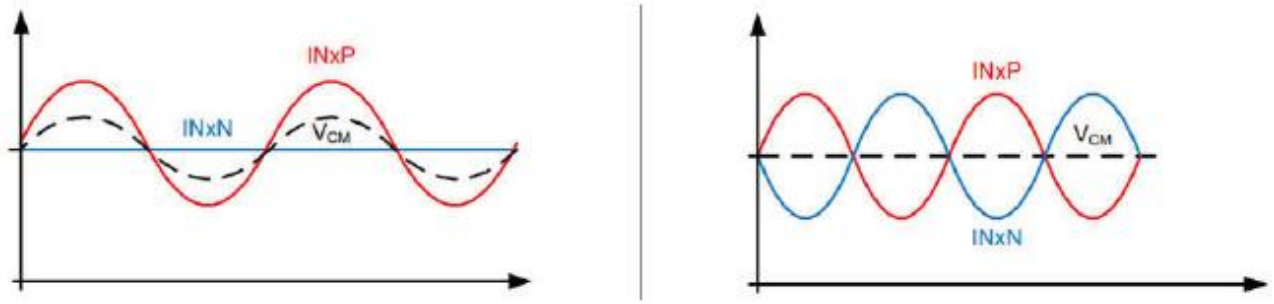


Figure 9.3.3 Pseudo-Differential (Left) and Fully Differential (Right) Driving Configurations

Maintaining the INxN pin at a common voltage, ideally at the mid-supply level, constitutes a pseudo-differential input approach. The INxP pin is then swung around this common voltage between $-V_{REF}$/Gain and V_{REF}/Gain, while staying within the absolute maximum rating specifications. When configured for pseudo-differential mode, the common-mode voltage (VCM) will vary with the signal level changes, requiring that the differential signal at its minimum and maximum satisfy the common-mode input specification.Configuring the signals on INxP and INxN as inverse signals centered around a common-mode voltage (VCM) represents the fully differential input method. Both INxP and INxN inputs swing from a common voltage of +½ VREF/Gain to a common voltage of –½ VREF/Gain. The differential voltage at the peaks and troughs equals $-V_{REF}$/Gain to VREF/Gain, centered around a fixed common-mode voltage. For optimal performance, it is recommended to set the common-mode voltage at the midpoint of the analog supplies, i.e., [(AVDD + AVSS)/2].

PGA settings and input range

The low-noise PGA is a differential-input and output amplifier whose gain settings (1, 2, 4, 6, 8, 12, and 24) can be configured by writing to the CHnSET register. As the CBM24AD98Q inputs are CMOS-based, current noise can be considered negligible. Table 9.3.1 presents typical bandwidth values for various gain settings. Please note that the table illustrates small-signal bandwidth; for large signals, performance is limited by the PGA's slew rate.

Table 9.3.1 PGA Gain and Bandwidth

Obtain	**Nominal bandwidth at room temperature (kHz)**
1	662
2	332
4	165
6	110
8	83

12	55
24	27

To maintain operation within the linear range of the PGA, input signals must comply with the following:

AVDD-0.2V-((Gain x V_{MAX_DIFF}))/2>CM>AVSS+0.2V+((Gain x V_{MAX_DIFF}))/2

Here, V_{MAX_DIFF} denotes the maximum differential input voltage of the PGA; CM represents the common-mode range. For instance: If AVDD = 5 V, Gain = 12, and VMAX_DIFF = 350 mV, then 2.3 V < CM < 2.7 V. The differential input voltage range (VINxP − VINxN) is dependent on the analog supply and reference voltage used in the system as well as the gain, spanning from −VREF/Gain to VREF/Gain.

ΔΣ Modulator

Each channel in the CBM24AD98Q features a 24-bit ΔΣ Analog-to-Digital Converter (ADC). The converter utilizes a second-order modulator optimized for low-noise applications. The modulator samples the input signal at a rate of (fMOD = fCLK/2), with the chip noise being shaped up to fMOD/2, as illustrated in Figure 9.3.4.

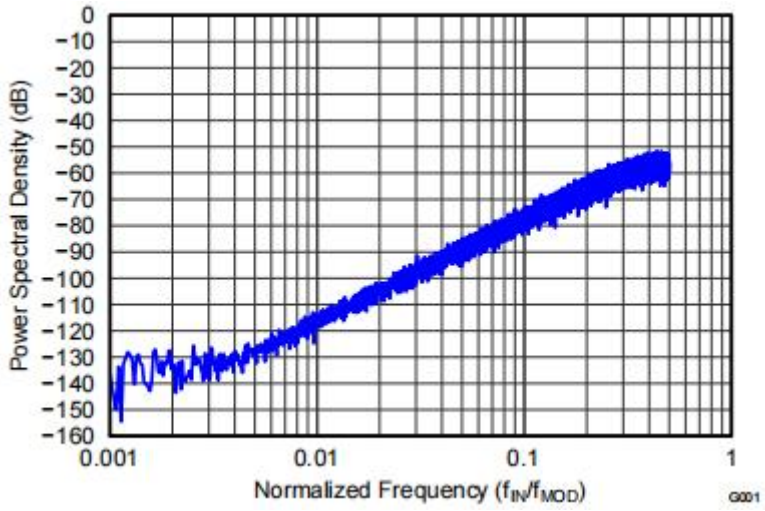


Figure 9.3.4 Modulator noise spectrum

Reference Voltage

The CBM24AD98Q internally generates a reference voltage typically at 4.5V or 2.4V (based on AVSS), controlled by the VREF_4V bit in the CONFIG3 register. When utilizing the internal reference voltage, VREFN should be connected to AVSS. The internal reference buffer can be disabled, allowing for the application of an external reference to VREFP. Figure 9.3.5 depicts a typical circuit for driving an external reference. The internal reference circuit can be powered down via the PD_REFBUF bit in the CONFIG3 register. In scenarios where multiple chips are

cascaded, the internal reference of one chip can be shared by powering it down on the others. By default, upon wake-up, the chip operates using an external reference.

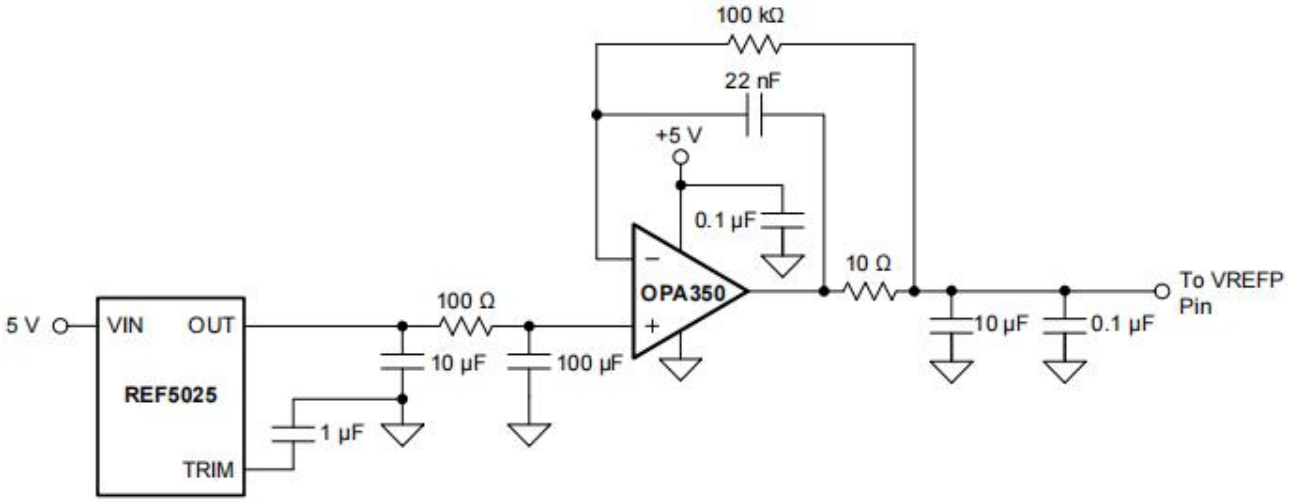


Figure 9.3.5 External Reference Driver

Digital decimation filter

The digital filter receives the modulator output and decimates the data stream. By adjusting the filtering parameters, a trade-off can be made between resolution and data rate: more filtering yields higher resolution, whereas less filtering allows for a higher data rate. Higher data rates are typically employed in EEG applications for AC lead-off detection. The digital filter on each channel comprises a third-order sinc filter. The decimation ratio of the sinc filter can be adjusted via the DR bits in the CONFIG1 register. This setting is a global one affecting all channels, hence all channels in the chip operate at the same data rate. The sinc filter is a third-order low-pass filter with a variable decimation rate. Data enters the filter at the rate of f_{MOD} from the modulator, undergoes high-frequency noise filtering, and is then decimated into parallel data at the rate of fDR. The Z-domain transfer function of the sinc filter (with N as the decimation factor) is as follows:

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3$$

Figure 9.3.6/7 shows the transmission characteristics of the filter, with normalized frequency on the horizontal axis and gain (dB) on the vertical axis.

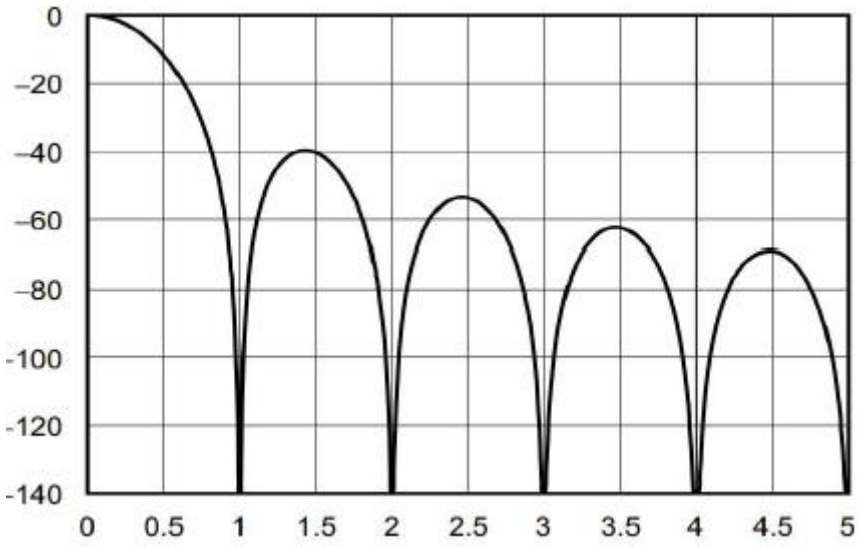


Figure 9.3.6 Sinc transmission characteristics (frequency normalized by f_{IN}/f_{DR})

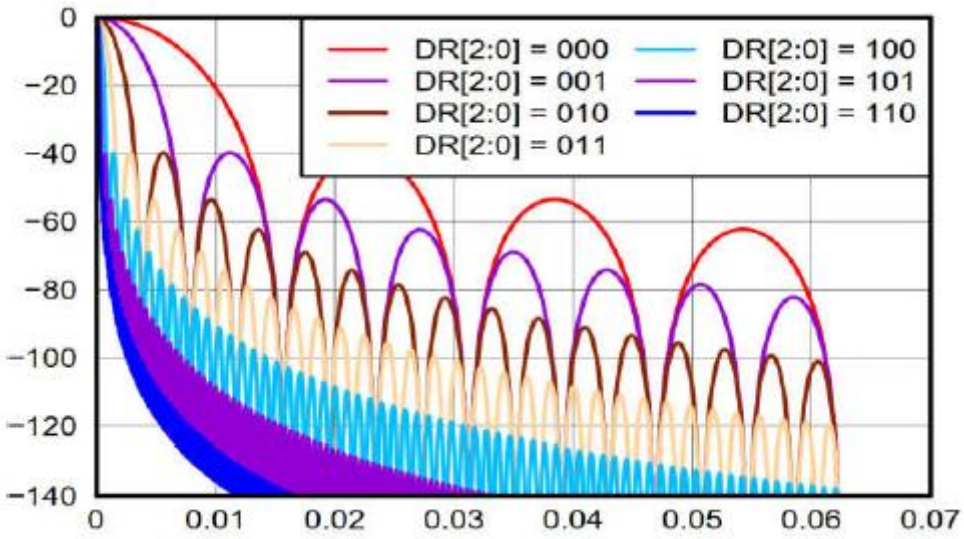


Figure 9.3.7 Sinc Filter Transfer Characteristics (Frequency Normalized to f_{IN}/f_{MOD})

Clock

The CBM24AD98Q offers both internal and external clocking methods. The internal clock is suitable for low-power, battery-operated systems, with the oscillator factory-calibrated at room temperature for accuracy. Clock selection is governed by the CLKSEL pin and the CLK_EN register bit.The CLKSEL pin determines whether the internal or external clock is used. The CLK_EN bit in the CONFIG1 register enables or disables the oscillator clock to be output on the CLK pin. A truth table for these two controls is provided in Table 9.3.2.

Table 9.3.2 Truth Table for CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG1.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	Tri-state
1	1	Internal clock oscillator	Output: internal clock oscillator

General-Purpose Input/Output Interface

The CBM24AD98Q features four general-purpose digital I/O (GPIO) pins available during normal operation modes. These GPIO pins can be individually configured as inputs or outputs via the GPIOC bit registers. The GPIO level is controlled by the GPIOD bits in the GPIO register. Reading the GPIOD bits returns the logical level of the pin, regardless of whether they are programmed as inputs or outputs. Writing to the GPIOD bits is ineffective when the GPIO pins are configured as inputs. When set as outputs, writing to the GPIOD bits sets the GPIO output value.

Bias (BIAS) Drive Circuit

Employing a bias (BIAS) drive circuit to stimulate the body helps counteract common-mode interference in EEG systems caused by power lines and other sources, including fluorescent lighting. Figure 9.3.8 illustrates an example of a bias circuit connection. The reference voltage for the bias drive can be internally generated [(AVDD + AVSS)/2] or externally supplied via a resistor divider network. Selection of the bias loop's reference voltage, either internal or external, is defined by writing the appropriate value to the BIASREF_INT bit in the CONFIG2 register. The BIAS_SENSEP/N selects the corresponding channel to be connected to the BIASINV terminal of the bias circuit. Upon choosing the appropriate channel, feedback components, and closing the loop externally on the chip, a BIAS bias signal is outputted at the BIASOUT pin. This signal can be fed, after filtering or directly, into the BIASIN pin, as depicted in Figure 9.12. To route this BIASIN signal to the designated input P-side/N-side electrode, the MUX bits in the respective channel setting register must be set to “110” / “111”.

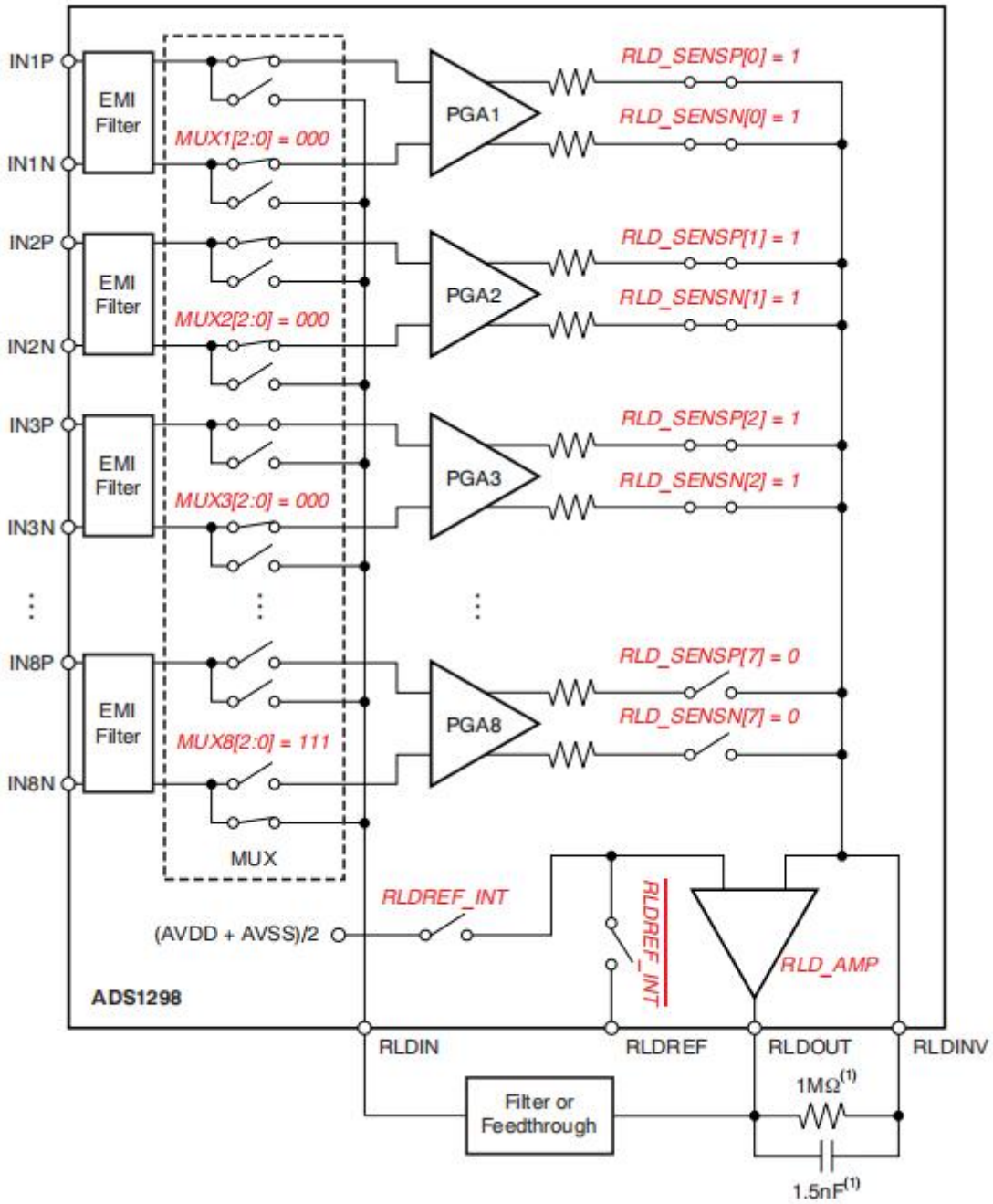


Figure 9.3.8. Example of RLDOUT Signal Configured to be Routed to IN8N

The bias drive functionality can be disabled using the PD_BIAS bit in the CONFIG3 register. When multiple CBM24AD98Q chips are daisy-chained, the PD_BIAS bit is used to disable all but one of the bias amplifiers. Figure 9.3.9 demonstrates the setup with multiple chips connected for the bias circuit. When several CBM24AD98Q chips are cascaded in a daisy chain configuration, it's essential to manage the bias amplifiers carefully. By leveraging the PD_BIAS bit found within the CONFIG3 register, you can selectively deactivate the bias amplifiers in all but one of the

interconnected devices. This ensures that only a single bias amplifier remains operational, which is typically sufficient for driving the bias current through the entire chain of chips. Figure 9.3.9 provides a visual representation of how these multiple chips are connected in relation to the bias circuit, highlighting the importance of proper bias amplifier management in multi-chip setups.

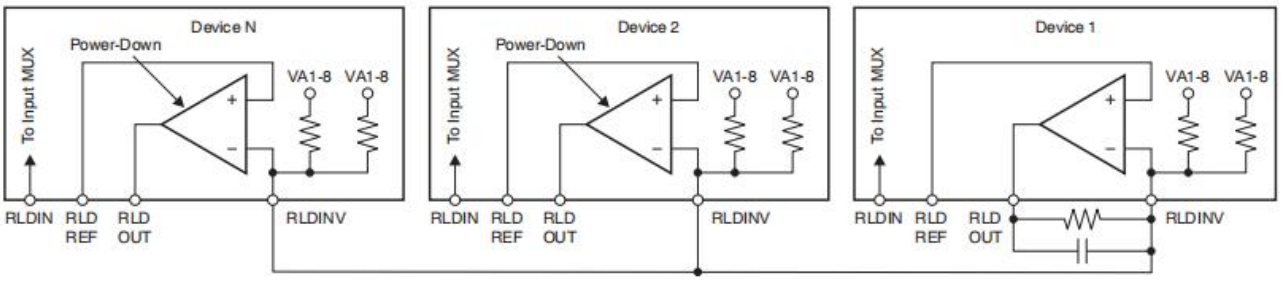


Figure 9.3.9 BIAS driver connections for multiple chips

Furthermore, the BIASOUT signal can be routed to a specific channel (not involved in the BIAS computation) for measurement purposes. Figure 3.9.10 illustrates the register settings required to route the BIASIN signal to Channel 8. The measurement is performed relative to the voltage on the BIASREF pin. If BIASREF is selected as internal, then BIASREF equals [(AVDD + AVSS)/2]. This feature can be utilized for debugging purposes during product development.Please note that Figure 3.9.10 was referenced as an illustrative example, but the actual figure content was not provided. The described functionality allows for the monitoring and verification of the BIASOUT signal's integrity and performance by measuring it against a known reference voltage, which is particularly useful during the prototyping and testing phases of product development.

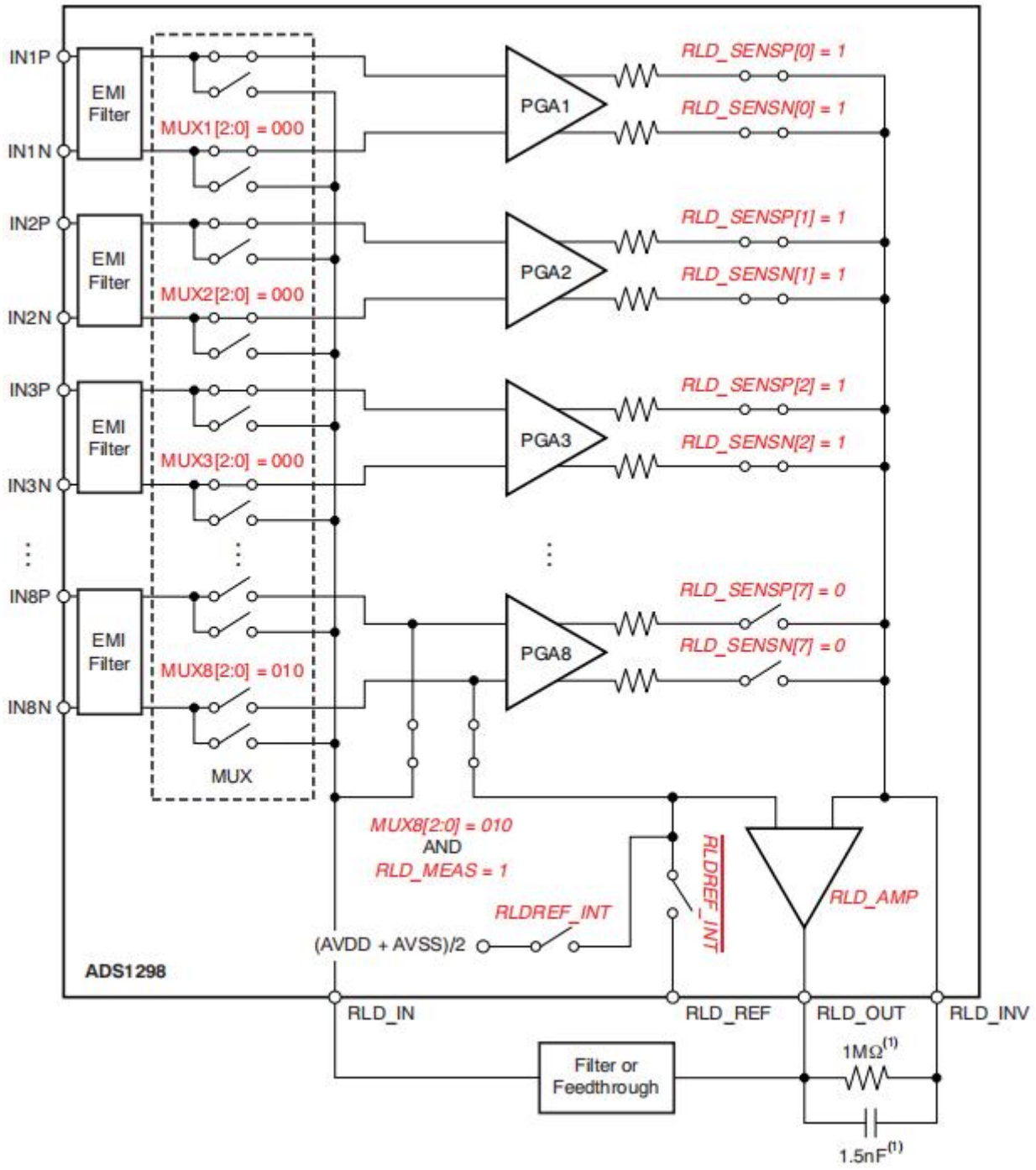
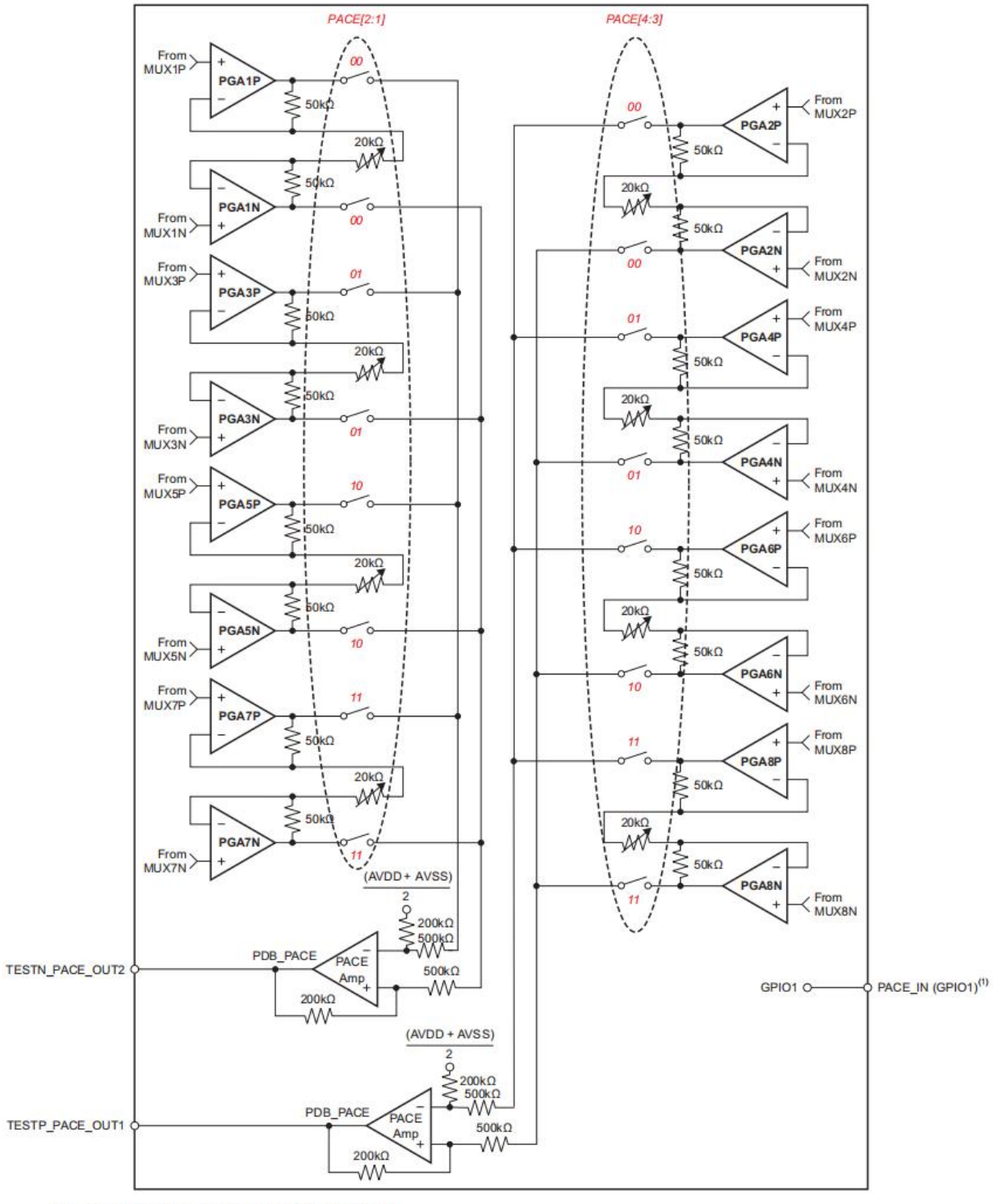


Figure 9.3.10. RLDOUT Signal Configured to be Read Back by Channel 8

In addition to the BIASOUT signal, which can serve as a reference for single-ended inputs in the CBM24AD98Q, there are also two Stimulus Reference (SRB1/2) signals that can act as references for single-ended inputs. These two signals further double as sensing signals for pacemakers. Figure 9.3.11 depicts the driving circuits for these signals. SRB2 is driven by the odd-numbered channels, and SRB1 by the even-numbered channels, with channel selection governed

respectively by the SRB2_SEL and SRB1_SEL register bits, detailed in the MISC1 register definition. Note that a 0.4 attenuation exists when converting from differential to single-ended, thus the total gain equals (0.4 × PGA_GAIN). Unlike BIASOUT, the SRB1/2 signal drivers are internally closed-looped within the chip, enabling direct use without requiring external closed-loop circuits.Regarding SRB1, it can only be routed to the negative end (N-end) of all channels under the control of the SRB1 bit in the MISC1 register, with the signal entering through the positive end (P-end), forming a differential input with SRB1.As for SRB2, it can be directed to the positive end (P-end) of the respective channel by the SRB2 bit in the corresponding CHnSET register of that channel, with the signal entering from the negative end (N-end), thereby creating a differential input with SRB2. It is important to note that the phase of the signal sampled and output after entering from the negative end will be inverted.



(1) GPIO1 can be used as the PACE_IN signal.

Figure 9.3.11 Excitation and Reference (SRB1/2) Drive Circuit

Lead-off Detection (Electrode Disconnection Detection)

The contact impedance between electrodes and the human body may change over time or during usage, leading to disconnections, necessitating continuous monitoring of the electrode-to-body connection. The CBM24AD98Q features a lead-off detection module designed specifically for this purpose. Although referred to as lead-off detection, it essentially detects electrode detachment.Fundamentally, lead-off detection works by injecting an excitation current and measuring the voltage to ascertain the quality of electrode contact, as illustrated in Figure 9.3.12. The circuitry provides two distinct methods for determining the status of the electrodes, differing primarily in the frequency components of the excitation signal. The leads to be monitored can be selected using the LOFF_SENSP and LOFF_SENSN registers.The first method involves stimulating the lead with a DC signal. The DC stimulation signal can originate from external pull-up or pull-down resistors or from an internal current source or sink, as shown in Figure 9.3.12. One side of the channel is pulled up to the supply voltage, while the other is pulled down to ground. By setting the corresponding bits in the LOFF_FLIP register, the pull-up and pull-down currents can be swapped. If a current source is used, the magnitude of the current can be set using the ILEAD_OFF[1:0] bits in the LOFF register. Compared to a 10-MΩ pull-up or pull-down resistor, a current source offers a higher input impedance.

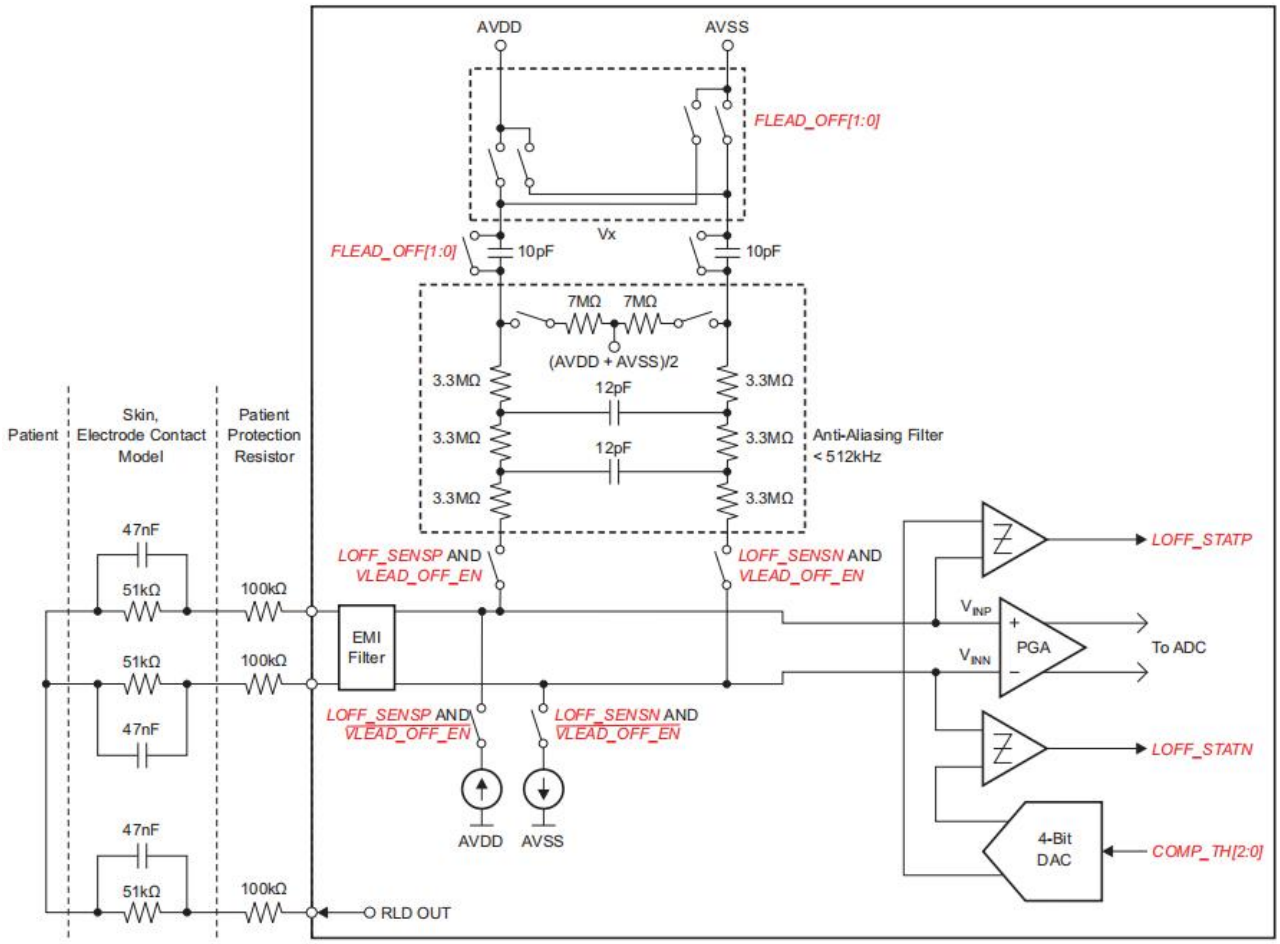


Figure 9.3.12. Lead-Off Detection

The connection status of the leads can be monitored by reading the output code of the channel or by employing an on-chip comparator. Should the electrode become disconnected, the pull-up and pull-down resistances cause the channel to saturate. The comparator monitors the input voltage against a 3-bit DAC level, with the DAC level set by the COMP_TH[2:0] bits in the LOFF register. The output of the comparator is stored in the LOFF_STATP and LOFF_STATN registers. This data forms part of the output data stream. (Refer to the Output Data section for more details.) If DC lead-off detection is not in use, the comparators can be deactivated by setting the PD_LOFF_COMP_ bit in the CONFIG4 register.

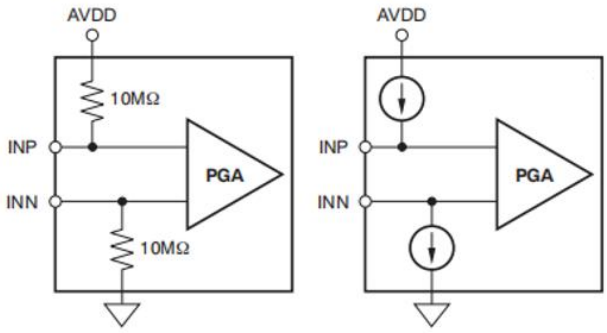


Figure 9.3.13 DC lead detachment detection options

Another approach employs an in-band AC signal to stimulate the leads. The AC signal is generated by alternately providing a fixed-frequency current source at the input. The frequency can be selected using the FLEAD_OFF[1:0] bits in the LOFF register (either 7.8 Hz or 31.2 Hz). This in-band excitation signal is captured through the channel and read at the output. The AC excitation introduces a frequency within the band of interest, which can be filtered and processed separately. The impedance of the electrodes can be calculated by measuring the output amplitude at the frequency of the excitation signal. For continuous lead-off detection, an out-of-band AC current can be applied externally to the input and digitally processed to determine electrode impedance.

9.3.12 Bias Drive (BIAS) Lead-off Detection

During normal operation of the CBM24AD98Q, right leg drive (RLD) lead-off detection cannot be utilized since the detection requires the disabling of the right leg drive amplifier. As depicted in Figure 9.3.14, the CBM24AD98Q employs a current source and a comparator to ascertain the connection state of the BIAS electrode. When the BIAS amplifier is powered on, the current source is inactive. The acceptable threshold for BIAS impedance can be determined by setting the reference level of the comparator, which is set in a manner identical to the threshold setting for other negative input signals, using the LOFF[7:5] bits. This threshold setting allows for the determination of the BIAS electrode's connectivity status.

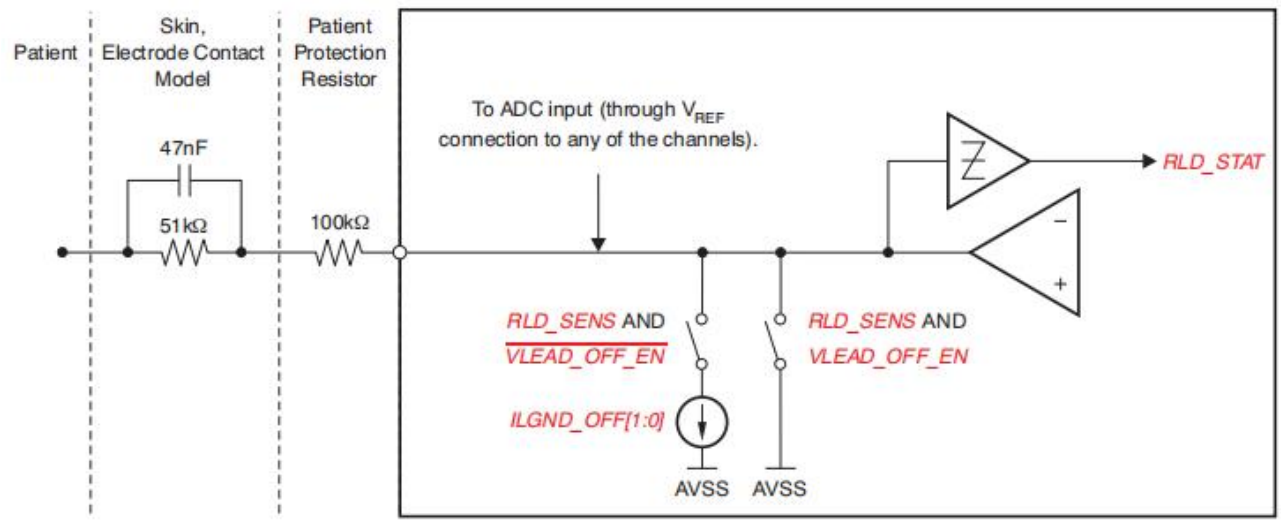


Figure 9.3.14. RLD Lead-Off Detection at Power Up

Wilson Central Terminal (WCT) and Augmented Leads

In a standard 12-lead ECG, the WCT voltage is defined as the average potential of the right arm (RA), left arm (LA), and left leg (LL) electrodes. This voltage serves as the reference voltage for measurements of the precordial leads. Integrated within the CBM24AD98Q chip are three low-noise amplifiers capable of generating the WCT voltage, as illustrated in Figure 9.3.15. Any one of the eight signals (from IN1P through IN4N) can be routed to each of these amplifiers to compute the average. This versatility enables the RA, LA, and LL electrodes to be connected to any input of the first four channels, depending on the lead configuration adopted. The adaptive design accommodates various lead setups while maintaining the essential function of the WCT as a stable reference point for electrocardiographic readings.

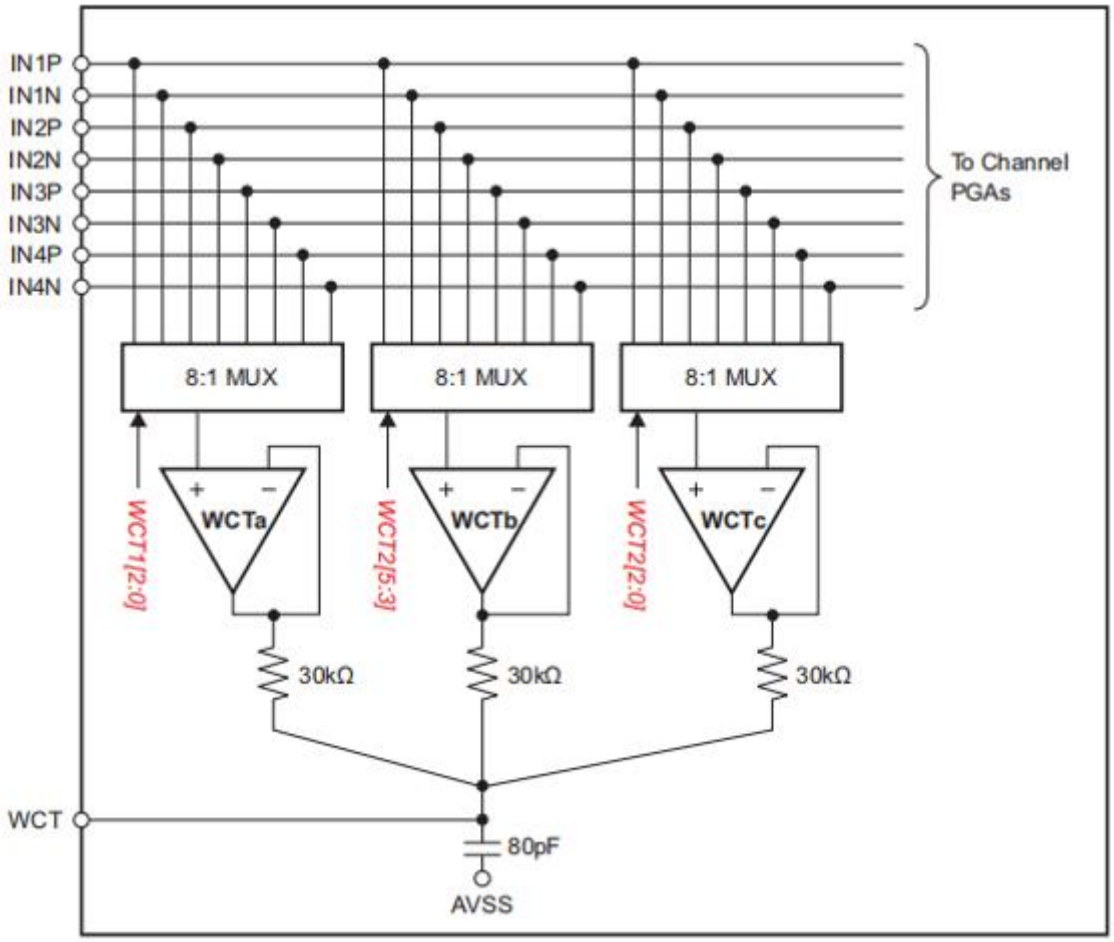


Figure 9.3.15 WCT lead generation circuit

Each of the three amplifiers in the WCT circuit can be individually powered down via register settings. By powering two amplifiers, the average potential of any two electrodes can be generated at the WCT pin. Notably, the drive strength of the WCT amplifiers is limited; thus, if they are utilized to drive low-impedance loads, buffering is advisable.Upon powering multiple WCT amplifiers, the overall noise level decreases, as depicted in Table 9.3.3. This noise reduction phenomenon arises from the averaging effect achieved by the passive summation network at the amplifier outputs. Power savings from disabling buffers are negligible, primarily due to a significant portion of the circuitry being shared among the three amplifiers.The bandwidth of the WCT node is constrained by an RC network. Internally, the summation network consists of three 30kΩ resistors and an 80pF capacitor. For optimal performance, an external 100pF capacitor is recommended to be added. The effective bandwidth is dependent on the number of amplifiers that are active.The WCT node can drive extremely high input impedances, typically exceeding 500MΩ. A common application involves connecting this WCT signal to the negative input terminal of the CBM24AD98Q, serving as the reference signal for precordial leads.

Table 9.3.3: Typical WCT Performance with 1, 2, or 3 Buffers Enabled、

This table outlines the variations in WCT performance characteristics when employing one, two, or all three of the available buffers, highlighting key metrics such as noise level, power consumption, and effective bandwidth under different operational configurations.

PARAMETER	ANY ONE (A, B, or C)	ANY TWO (A+B, A+C, or B+C)	ALL THREE (A+B+C)	UNIT
Integrated noise	540	382	312	nV_{RMS}
Power	53	59	65	µW
–3-dB BW	30	59	89	kHz
Slew rate	BW limited	BW limited	BW limited	V/µs

As previously mentioned, all three WCT amplifiers can be connected to any one of the eight analog input pins. The inputs to these amplifiers are subject to chopper modulation, with the chopping frequency varying according to the data rate setting of the CBM24AD98Q. The chopping frequencies for the three highest data rates maintain a 1:1 ratio. For instance, at a data rate of 32k samples per second (32kSPS) in HR mode, the chopping frequency is 32kHz when WCT_CHOP is set to 0. Conversely, the chopping frequencies for the four lower data rates are fixed at 4kHz. When WCT_CHOP is set to 1, the chopping frequency is locked to the highest data rate frequency, specifically fMOD/16, as illustrated in Table 9.3.4.This out-of-band chopping does not interfere with ECG-related measurements. However, if a channel connected to a WCT amplifier, such as the V lead channel, has its output linked to a pacing signal amplifier used for detecting external pacing signals, chopper artifacts may become evident at the output of the pacing signal amplifier.

Table 9.3.4: WCT Chopping Frequencies

CONFIG1.DR[2:0] BIT	CONFIG2.WCT_CHOP = 0	CONFIG2.WCT_CHOP = 1
000	f_{MOD}/16	f_{MOD}/16
001	f_{MOD} / 32	f_{MOD} / 16
010	f_{MOD} / 64	f_{MOD} / 16
011	f_{MOD} / 128	f_{MOD} / 16
100	f_{MOD} / 128	f_{MOD} / 16
101	f_{MOD} / 128	f_{MOD} / 16
110	f_{MOD} / 128	f_{MOD} / 16

In a typical 12-lead ECG application with eight channels, augmented leads are computed digitally. However, there may be instances where all leads, including the augmented ones, are required to be derived in an analog (as opposed to digital) form. The CBM24AD98Q offers the option to generate these augmented leads by routing the respective averages to Channels 5, 6, and 7. The same three amplifiers utilized for creating WCT signals are also employed in generating the Wilson Central Terminal (WCT) signal.Figure 9.3.16 illustrates an example of generating

augmented leads in the analog domain. More than eight channels are utilized in this depiction to produce the standard 12 leads; hence, this functionality is not available on the CBM24AD98Q-4 or CBM24AD98Q-6 variants. This highlights a scenario where additional hardware capabilities facilitate the analog derivation of all necessary ECG leads directly, bypassing the need for digital post-processing for the augmented leads.

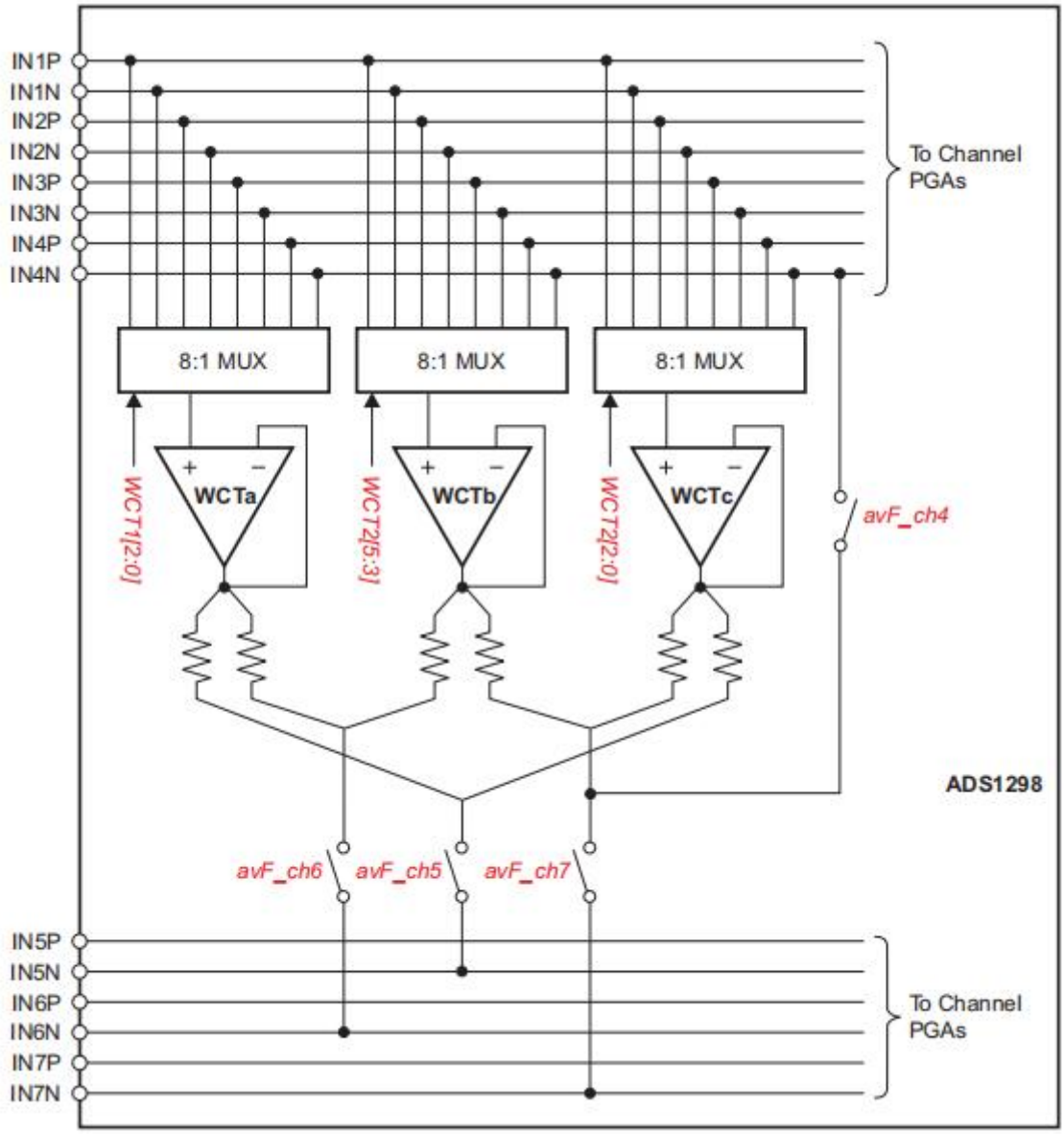


Figure 9.3.16 Enhanced leads

Product Function Modes

Product Function Modes

Start (START)

Initiating a conversion can be achieved by pulling the START pin high for at least 2 tCLK cycles, or by issuing a START command. When START is low and no START command has been transmitted, the chip does not assert the DRDY_ signal (conversion is paused). When utilizing the START command to control conversions, maintain the START pin at a low level. The CFYA98 features two operational modes for controlling conversions: Continuous mode and Single-shot mode, which is selected by the SINGLE_SHOT bit (bit 3 of the CONFIG4 register). In multi-chip configurations, the START pin serves to synchronize the chips.The settling time (tSETTLE) refers to the duration required for output data to become fully stable after the analog-to-digital conversion begins. Upon the assertion of START, DRDY_ is also pulled high. The subsequent falling edge of DRDY_ signifies that the data is ready. Figure 9.4.1 illustrates the timing diagram, while Table 9.4.1 lists the settling times for various data rates.The settling time depends on fCLK and the decimation rate (controlled by the DR[2:0] bits in the CONFIG1 register). Following the initial settling period, DRDY_ goes low, indicating that the data conversion is complete and will appear at the set data rate tDR. If data is not read back from DOUT before the next conversion is ready, DRDY_ goes high for 4 tCLK periods before returning low, signaling new data readiness.Note that when START remains high and there is a step change in the input signal, the filter requires 3×tDR to stabilize to the new value. Stable data is then ready at the fourth DRDY_ falling edge.

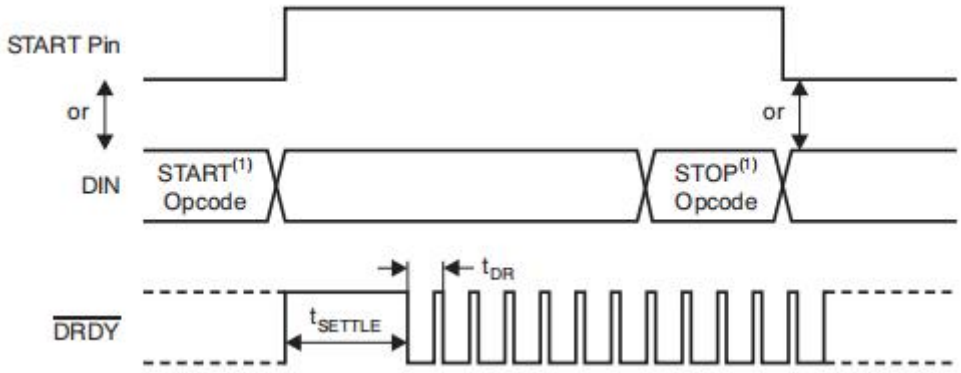


Figure 9.4.1 Stability time

Table 9.4.1 Establishment time for different data rates

DR[2:0]	Normal mode	Unit
000	521	t_{CLK}
001	1033	t_{CLK}

010	2057	t_{CLK}
011	4105	t_{CLK}
100	8201	t_{CLK}
101	16393	t_{CLK}
110	32777	t_{CLK}

Reset (RESET_)

There are two methods to reset the CBM24AD98Q: by pulling the RESET_ pin low or by sending a RESET command. When using the RESET_ pin, ensure compliance with the minimum pulse duration timing specification before pulling the pin back high. The RESET command takes effect on the eighth falling edge of SCLK after the command is issued. Following a reset, 18 tCLK cycles are required to initialize configuration registers to their default states and commence the conversion cycle. Note that an internal reset to the digital filter is automatically issued when the CONFIG1 register is set to a new value using the WREG command.9.4.3 Power-Down (PWDN_) All on-chip circuits are shut off when the PWDN_ pin is pulled low. To exit power-down mode, the PWDN_ pin should be pulled high. After exiting power-down mode, the internal oscillator and reference require time to wake up. It is recommended to disable the external clock during power-down to conserve power.

Data Acquisition

(1) Data Ready (DRDY_)

DRDY_ is an output signal that transitions from high to low to indicate new conversion data is ready. The CS_ signal has no effect on the data ready signal. The behavior of DRDY_ depends on whether the chip is in RDATAC mode, continuously outputting data, or using RDATA commands for on-demand data reads. When reading data with the RDATA command, the read operation can overlap with the next DRDY_ without data corruption. The START pin or START command places the chip into either normal data capture mode or pulsed data capture mode.Figure 9.4.2 illustrates the relationship between DRDY_, DOUT, and SCLK during data read operations. DOUT is latched on the rising edge of SCLK, and DRDY_ is pulled high on the falling edge of SCLK. Note that DRDY_ goes high on the first falling edge of SCLK, regardless of whether data is being read or commands are being sent via the DIN pin.

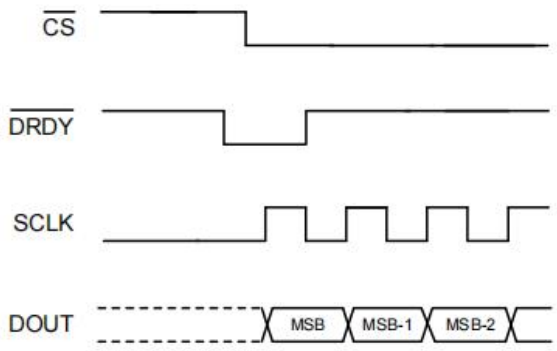


Figure 9.4.2 DRDY_ with data retrieval (CS=0)

(2)Data Readout

Data readout can be accomplished through one of the following two methods:

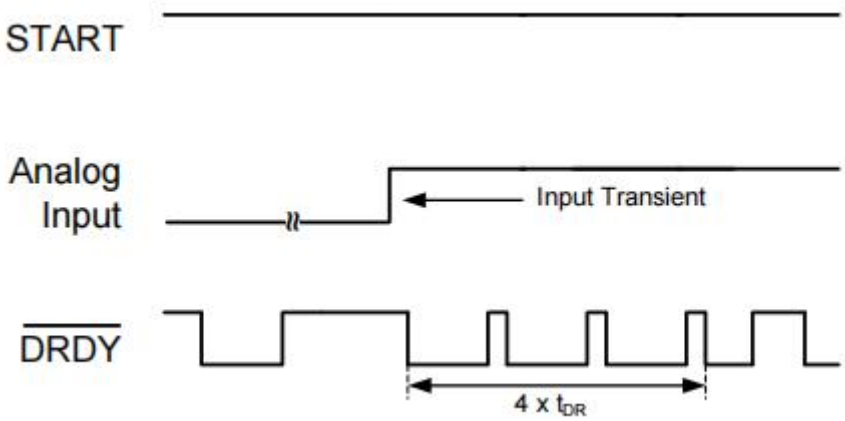
1. RDATAC: The Continuous Data Read Command sets the chip into continuous read mode, where new data is automatically loaded into the output shift register upon completion of each data conversion without the need to send a command. For more detailed information, refer to the RDATAC: Continuous Data Read section.

2. RDATA: The Data Read Command requires sending a command to the chip to load the latest data into the output shift register. For more detailed information, see the RDATA: Data Read section.Conversion data is read out by shifting data out on DOUT. The MSB of the data on DOUT is output on the first rising edge of SCLK. DRDY_ returns high on the first falling edge of SCLK for the entire read operation. DIN should remain low for the duration of the read operation.The number of bits in the data output depends on the number of channels and the number of bits per channel. For an 8-channel CBM24AD98Q, the amount of data output is [24 status bits + (24 bits x 8 channels) = 216 bits]. The format of the 24 status bits is: (1100 + LOFF_STATP + LOFF_STATN + bits [4:7] of the GPIO register). The data format for each channel is a two’ s complement binary format with the MSB first. When channels are turned off using user register settings, the corresponding channel output is set to "0". However, the order of channel outputs remains unchanged.The CBM24AD98Q also offers multireadback functionality. By simply providing more SCLKs in RDATAC mode, data can be read multiple times, in which case the MSB data byte repeats after reading the last byte. For multireadback, the DAISY_EN_ bit in the CONFIG1 register must be set to "1".

9.4.5 Continuous Conversion Mode

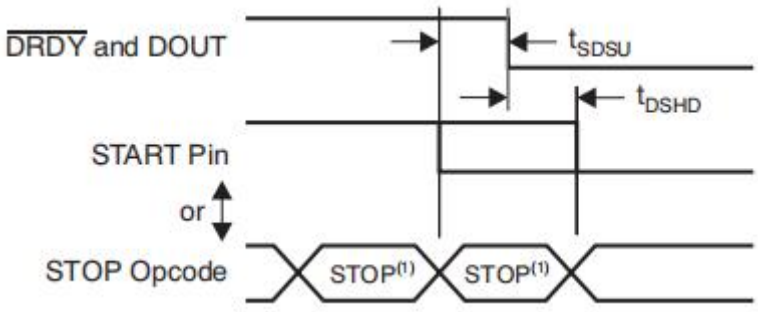
Conversions begin when the START pin is pulled high or a START command is sent. As shown in Section 9.4.3, the DRDY_ output goes high when the conversion starts and goes low when the

data is ready. Conversions will continue indefinitely until the START pin goes low or a STOP command is sent. When the START pin is pulled low or a STOP command is issued, the currently ongoing conversion is allowed to complete. Figures 9.4.4 and Table 9.4.2 depict the timing of the START pin or the START and STOP commands to the DRDY_ signal during data conversion. tSDSU indicates when the START pin should be pulled low or when the STOP command should be sent before the falling edge of DRDY_ to halt further conversions. tDSHD indicates when the START pin should be pulled low or when the STOP command should be sent after the falling edge of DRDY_ to complete the current conversion and halt further conversions. To keep the converter running continuously, the START pin can be kept high.When switching from Single-Shot mode to continuous conversion mode, pull the START signal low then high again, or send a STOP command followed by a START command. This conversion mode is suitable for applications requiring a fixed, continuous stream of conversions.



**The START and STOP commands take effect on the 7th falling edge of SCLK.

Figure 9.4.3 Continuous Conversion Mode



The START and STOP commands take effect on the seventh falling edge of the SCLK at the end of the command.

Figure 9.4.4 Start to DRDY timing

Table 9.4.2 Time series characteristics

		MIN	MAX	UNIT
t_{SDSU}	START pin low or STOP opcode to $\overline{DRDY}$ setup time to halt further conversions	16		t_{CLK}
t_{DSHD}	START pin low or STOP opcode to complete current conversion	16		t_{CLK}

9.4.6 Single-Shot Mode

Single-shot mode is enabled by setting the SINGLE_SHOT bit in the CONFIG4 register to "1". In single-shot mode, the CBM24AD98Q performs a single conversion when the START pin is pulled high or a START command is issued. As illustrated in Figure 9.4.5, upon completion of the conversion, DRDY_ goes low and halts further conversions. DRDY_ remains low regardless of whether the conversion data is read or not. To initiate a new conversion, the START pin must be pulled low and then high again, or the START command must be resent. When transitioning from continuous conversion mode to single-shot mode, the START signal should be pulled low and then high again, or a STOP command should be issued before sending another START command.

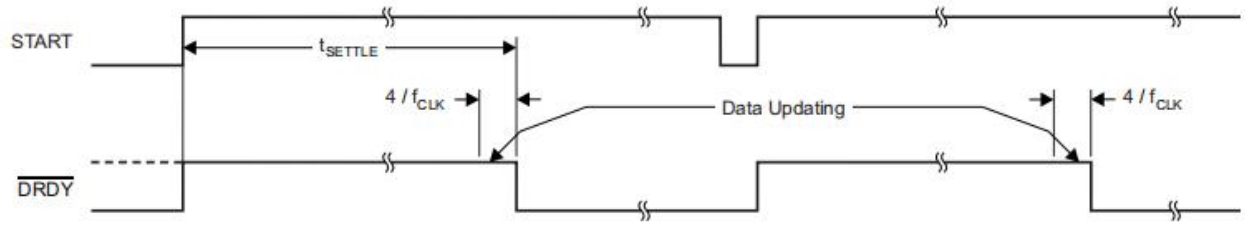


Figure 9.4.5 DRDY_ No Data Recovery in SingLE-SHOT Mode

This conversion mode is tailored for applications that require non-standard or non-continuous data rates. Issuing a START command or toggling the START pin high resets the digital filter, effectively quartering the data rate. This mode imposes a heavier load on the host processor, as it must toggle the START pin or issue START commands to initiate new conversion cycles.

9.5 Programming

9.5.1 Data Format

The chip represents 24-bit data in two's complement format. The size of a least significant bit (LSB) in terms of voltage is calculated using the following formula:

$$1\ LSB = (2 \times V_{REF} / Gain) / 2^{\wedge 24} = +FS / 2^{\wedge 23}$$

A full-scale positive input results in an output code of 7FFFFFh, whereas a full-scale negative input yields an output code of 800000h. For signals exceeding the full-scale range, the output clips at these codes. The table below summarizes the ideal output codes for various input signals.

Table 9.5.1 Ideal Output Code and Input Signal

INPUT SIGNAL, V_{IN} (INxP – INxN)	IDEAL OUTPUT CODE(2)
≥ V_{REF}	7FFFFFh
V_{REF} / (2^{23} – 1)	000001h
0	000000h
–V_{REF} / (2^{23} – 1)	FFFFFFh
≤ –V_{REF} (2^{23} / (2^{23} – 1))	800000h

9.5.2 SPI Interface

The SPI-compatible serial interface of the CBM24AD98Q is composed of four signals: CS_, SCLK, DIN, and DOUT, which are used for reading conversion data, reading and writing to registers, and controlling the operation of the CBM24AD98Q. The data-ready output DRDY_ acts as a status signal to indicate when data is ready, going low when new data becomes available.

Chip Select (CS_)

The CS_ pin activates SPI communication. CS_ must be low before data transfer and must remain low throughout the SPI communication cycle. When CS_ is high, the DOUT pin enters a high-impedance state, causing reads and writes to the serial interface to be ignored and resetting the interface. DRDY_ operates independently of CS_; it still indicates a new conversion is complete and forces high in response to SCLK even when CS_ is high. Setting CS_ high stops SPI communication and resets the serial interface. Data conversion continues, and DRDY_ can be monitored to check for readiness of new conversion results. A master device monitoring DRDY_ can select the appropriate slave chip by pulling CS_ low. After serial communication, wait for four or more tCLK cycles before pulling CS_ high.

Serial Clock (SCLK)

SCLK provides the clock for serial communication. SCLK is a Schmitt-trigger input, but a clean SCLK is advised to prevent glitches from inadvertently shifting data. Data is shifted into DIN on the falling edge of SCLK and out of DOUT on the rising edge.Ensure all SCLK clocks are sent to the chip when transmitting commands. Failure to do so may lead to an unknown state in the chip's SPI serial interface, requiring CS_ to be pulled high for recovery.For a single chip, the minimum SCLK speed depends on the number of channels, resolution bits, and output data rate. For multiple cascaded chips, the SCLK frequency must ensure all channels' data can be read within the data-ready intervals. Data acquisition is accomplished by placing the chip in RDATAC mode or issuing RDATA commands.

Data Input (DIN)

DIN, along with SCLK, is used to send data to the chip. Data on DIN is shifted into the chip on the falling edge of SCLK.Communication with the chip is inherently full-duplex. The chip monitors incoming commands even while data is shifting out. When sending commands, data from the output shift register is shifted out. Therefore, ensure anything sent on DIN during data output is valid. Send a NOP command on DIN when not sending commands to the chip during data reads.

Data Output (DOUT)

DOUT, in conjunction with SCLK, is used to read conversion and register data from the chip. Data is output on the rising edge of SCLK, with the MSB first. DOUT enters a high-impedance state when CS_ is high. Figure 9.5.1 illustrates the CBM24AD98Q data output protocol.

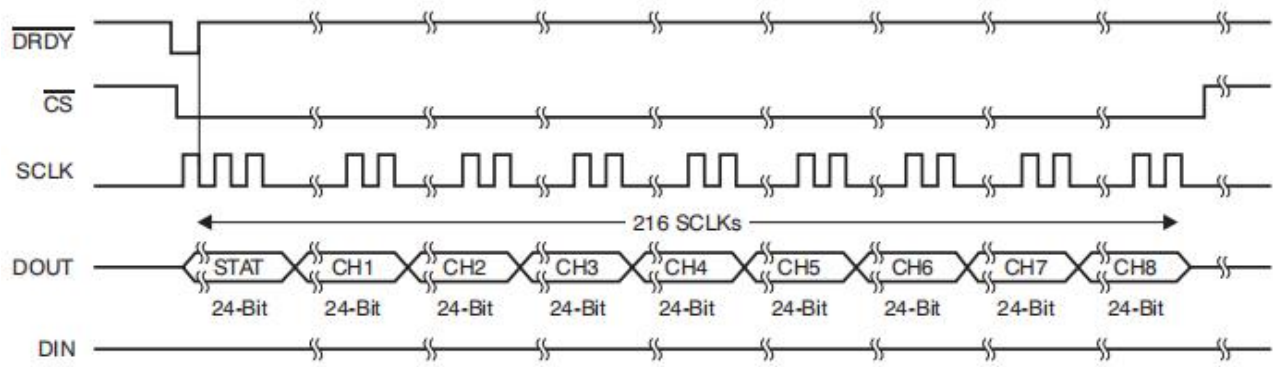


Figure 9.5.1 SPI Bus Data Output

The SPI command definitions for the CBM24AD98Q provide flexible configuration control. The operations for command control and configuring the chip are listed in Table 9.5.2. Except for register read and write operations, which require data appended to the second command byte, all other commands are standalone. CS_ can be released high or kept low between commands, but it must remain low throughout the entire command operation (especially for multi-byte commands). System commands and RDATA commands are decoded by the chip on the falling edge of the seventh SCLK. Register read/write commands are decoded on the falling edge of the eighth SCLK. When pulling CS_ high after issuing a command, make sure to follow the SPI timing requirements. Table 10. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
SYSTEM COMMANDS			
WAKEUP	Wakeup from standby mode	0000 0010 (02h)	—
STANDBY	Enter standby mode	0000 0100 (04h)	—
RESET	Reset the device	0000 0110 (06h)	—
START	Start/restart (synchronize) conversions	0000 1000 (08h)	—
STOP	Stop conversion	0000 1010 (0Ah)	—
DATA READ COMMANDS			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power up.(1)	0001 0000 (10h)	—
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	—
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	—
REGISTER READ COMMANDS			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn* (2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn* (2)

(1) In RDATAC mode, the RREG command will be ignored.

(2) n nnnn represents the number of registers to read or write minus one. For instance, to read or write three registers, set n nnnn to 0 (binary 0010). r rrrr denotes the starting register address for the read or write command.

(1) Sending Multi-Byte Commands

The CBM24AD98Q serial interface decodes commands byte by byte, requiring 4 tCLK cycles for decoding and execution. Therefore, when sending multi-byte commands (such as RREG or WREG), the end of one byte (or command) must be separated from the end of the next byte (or command) by 4 tCLK cycles. Assuming CLK is 2.048 MHz, then tSDECODE (4tCLK) is 1.96 μs. When SCLK is 16MHz, one byte can be transmitted within 500ns (0.5 μs). This byte transmission time does not meet the tSDECODE specification; therefore, a delay must be inserted so that the end of the second byte arrives after 1.46 μs. If SCLK is 4 MHz, then one byte is transmitted within 2 μs. Since this transmission time exceeds the tSDECODE specification, the processor can send subsequent bytes without delay.

(2) WAKEUP: Exit Standby Mode

The WAKEUP command exits the low-power standby mode. This command has no SCLK rate limit and can be issued at any time. Any subsequent commands must be sent after a delay of 4 tCLK cycles.

(3) STANDBY: Enter Standby Mode

The STANDBY command enters the low-power standby mode. All parts of the circuit except for the reference section are shut down. This command has no SCLK rate limit and can be issued at any time. After the chip enters standby mode, do not send any other commands except for the wakeup command.

(4) RESET: Reset Registers to Default Values

The RESET command resets the digital filter period and sets all registers back to their default values. This command has no SCLK rate limit and can be issued at any time. Executing the RESET command requires 18 tCLK cycles; avoid sending any commands during this period.

(5) START: Start Conversion

The START command initiates data conversion. The START pin needs to be pulled low to control the conversion through the command. If a conversion is already in progress, this command is invalid. The STOP command stops the conversion. If a START command is immediately followed by a STOP command, there must be a delay of 4 tCLK cycles between them. When sending the START command to the chip, keep the START pin low until the STOP command is issued. This command has no SCLK rate limit and can be issued at any time.

(6) STOP: Stop Conversion

The STOP command halts the conversion. Pull the START pin low to control the conversion via the command. When the STOP command is issued, the ongoing conversion completes and further conversions are stopped. If the conversion has already been stopped, this command is invalid. This command has no SCLK rate limit and can be issued at any time. (7) RDATAC: Continuous Read Data The RDATAC command initiates the output of conversion data on each DRDY_ without the need for subsequent read data commands. This mode places the conversion data in the output register, where it can be directly shifted out. The continuous read data mode is the default mode for the chip, which defaults to this mode upon power-up. The RDATAC mode is canceled by a stop read data continuously command. If the chip is in RDATAC mode, a SDATAC command must first be issued before any other commands can be sent to the chip. This command has no SCLK rate limit; however, subsequent data read SCLK or SDATAC commands should wait for at least 4 tCLK cycles before completion (see the section on sending multi-byte commands). The timing for RDATAC is shown in Figure 9.5.2, with a prohibited area of 4 tCLK cycles around the DRDY_ pulse where this command cannot be issued. To read data from the chip after issuing the RDATAC command, ensure that the START pin is high or issue a START command.

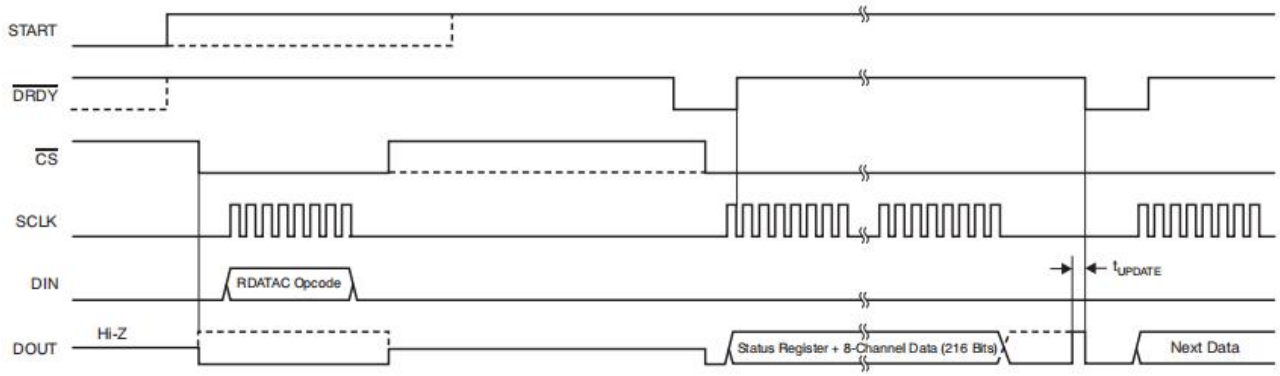


Figure 9.5.2 Usage of RDATAC command

(8) SDATAC: Stop Reading Data Continuously The SDATAC command cancels the continuous read data mode. This command has no SCLK rate limit, but the next command must wait for 4 tCLK cycles before completion. (9) RDATA: Read Data When not in continuous read data mode, the RDATA command loads the latest data into the output shift register. Issue this command after DRDY_ goes low to read the conversion result. This command has no SCLK rate limit, and no waiting time is required for subsequent commands or data read SCLKs. To read data from the chip after issuing the RDATA command, ensure that the START pin is high or issue a START command. When using the RDATA command to read data, the read operation can overlap with the next DRDY_ without corrupting the data. Figure 9.5.3 illustrates the usage of the RDATA command.

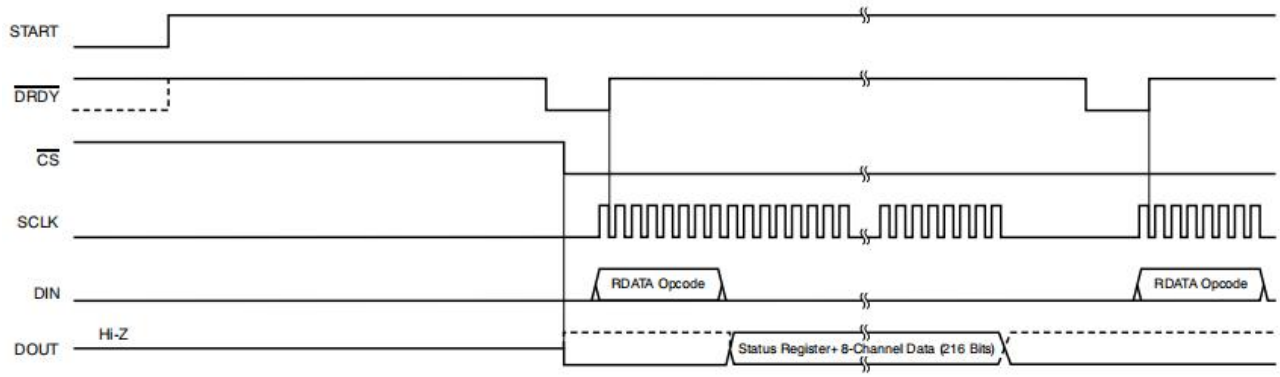


Figure 9.5.3 Usage of RDATA command

(10) RREG: Read Data from Register This command reads data from the register. The register read command is a two-byte command followed by the output of register data. The first byte contains the command and the register address. The second command byte specifies the number of registers to read, minus one. First command byte: 001r rrrr, where r rrrr is the starting register address. Second command byte: 000n nnnn, where n nnnn is the number of registers to read, minus one. The MSB of the first register is output on the 17th rising edge of SCLK, as shown in

Figure 9.5.4. When the chip is in continuous read data mode, an SDATAC command must be issued before the RREG command can be sent. The RREG command can be issued at any time. However, since this command is a multi-byte command, it has an SCLK rate limit due to the need to meet the tSDECODE timing for SCLK issuance. Note that CS_ must remain low throughout the entire command duration.

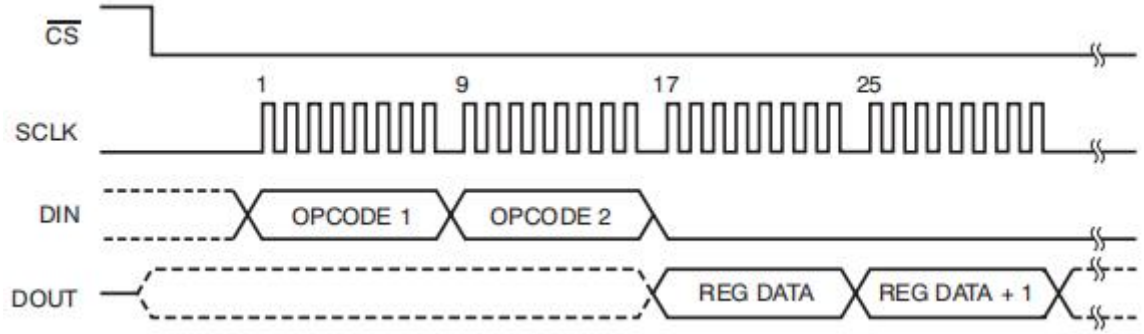


Figure 9.5.4 RREG command example: Starting from register 00h (ID register), read two registers (BYTE1=00100000, BYTE 2)=00000001)

(11) WREG: Write Data to Register This command writes data to the register. The register write command is a two-byte command followed by the input of register data. The first byte contains the command and the register address. The second command byte specifies the number of registers to write, minus one. First command byte: 010r rrrr, where r rrrr is the starting register address. Second command byte: 000n nnnn, where n nnnn is the number of registers to write, minus one. Following the command bytes is the register data (MSB-first format), as shown in Figure 9.5.5. The WREG command can be issued at any time; however, since this command is a multi-byte command, it has an SCLK rate limit due to the need to meet the tSDECODE timing for SCLK issuance. Note that CS_ must remain low throughout the entire command duration.

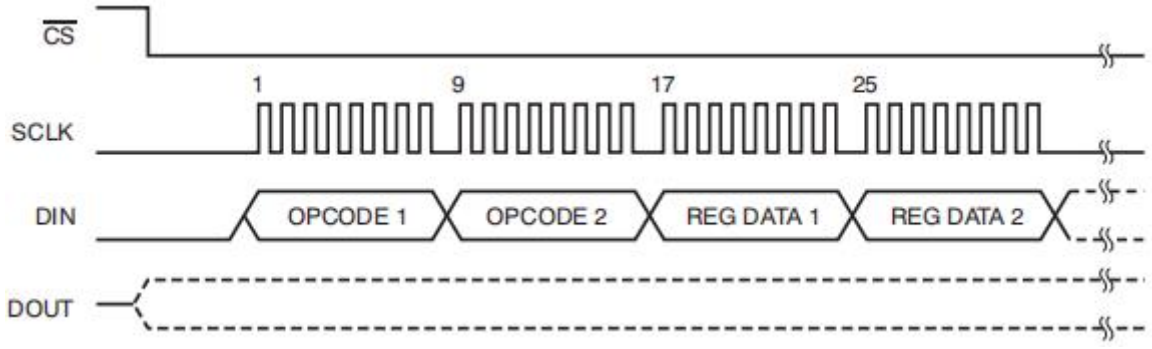


Figure 9.5.5 Example of WREG command: Starting from 00h (ID register), write two registers (BYTE 1=0100 0000, BYTE2=000000 1)

Register Definition

Register Definition

Table 9.6.1 illustrates the various CBM24AD98Q registers.

Table 9.6.1 Register Allocation

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE SETTINGS (READ-ONLY REGISTERS)										
00h	ID	xx	DEV_ID7	DEV_ID6	DEV_ID5	1	0	DEV_ID2	DEV_ID1	DEV_ID0
GLOBAL SETTINGS ACROSS CHANNELS										
01h	CONFIG1	06	HR	$\overline{\text{DAISY\_EN}}$	CLK_EN	0	0	DR2	DR1	DR0
02h	CONFIG2	40	0	0	WCT_CHOP	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0
03h	CONFIG3	40	$\overline{\text{PD\_REFBUF}}$	1	VREF_4V	RLD_MEAS	RLDREF_INT	$\overline{\text{PD\_RLD}}$	RLD_LOFF_SENS	RLD_STAT
04h	LOFF	00	COMP_TH2	COMP_TH1	COMP_TH0	VLEAD_OFF_EN	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0
CHANNEL-SPECIFIC SETTINGS										
05h	CH1SET	00	PD1	GAIN12	GAIN11	GAIN10	0	MUX12	MUX11	MUX10
06h	CH2SET	00	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20
07h	CH3SET	00	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30
08h	CH4SET	00	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40
09h	CH5SET (1)	00	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50
0Ah	CH6SET (1)	00	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60
0Bh	CH7SET (1)	00	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70
0Ch	CH8SET (1)	00	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80
0Dh	RLD_SENSP (2)	00	RLD8P(1)	RLD7P(1)	RLD6P(1)	RLD5P(1)	RLD4P	RLD3P	RLD2P	RLD1P
0Eh	RLD_SENSN (2)	00	RLD8N(1)	RLD7N(1)	RLD6N(1)	RLD5N(1)	RLD4N	RLD3N	RLD2N	RLD1N
0Fh	LOFF_SENSP (2)	00	LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P
10h	LOFF_SENSN (2)	00	LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N
11h	LOFF_FLIP	00	LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1
LEAD-OFF STATUS REGISTERS (READ-ONLY REGISTERS)										
12h	LOFF_STATP	00	IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF
13h	LOFF_STATN	00	IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF
GPIO AND OTHER REGISTERS										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1
15h	PACE	00	0	0	0	PACEE1	PACEE0	PACEO1	PACEO0	$\overline{\text{PD\_PACE}}$
16h	RESP	00	RESP_DEMOD_EN1	RESP_MOD_EN1	1	RESP_PH2	RESP_PH1	RESP_PH0	RESP_CTRL1	RESP_CTRL0
17h	CONFIG4	00	RESP_FREQ2	RESP_FREQ1	RESP_FREQ0	0	SINGLE_SHOT	WCT_TO_RLD	$\overline{\text{PD\_LOFF\_COMP}}$	0
18h	WCT1	00	aVF_CH6	aVL_CH5	aVR_CH7	avR_CH4	$\overline{\text{PD\_WCTA}}$	WCTA2	WCTA1	WCTA0
19h	WCT2	00	$\overline{\text{PD\_WCTC}}$	$\overline{\text{PD\_WCTB}}$	WCTB2	WCTB1	WCTB0	WCTC2	WCTC1	WCTC0

(1) Registers or bits are only available in the CBM24AD98Q-6 and CBM24AD98Q. In the CBM24AD98Q-4, the register bits are set to 0h or 00h.

(2) Registers or bits are only available in the CBM24AD98Q. In both the CBM24AD98Q-4 and CBM24AD98Q-6, the register bits are set to 0h.

9.6.1 Register Descriptions

The read-only ID control register is programmed during device manufacture to indicate device characteristics.

9.6.1.1 ID: ID Control Register (address = 00h) (reset = xxh)

7	6	5	4	3	2	1	0
DEV_ID[7:5]			1	0	DEV_ID[2:0]		
R-x			R-2h		R-x		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.2. ID Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEV_ID[7:5]	R	xh	**Device ID** These bits indicate the device family. 000 = Reserved 011 = Reserved 100 = ADS129x device family 101 = Reserved 110 = ADS129xR device family 111 = Reserved
4:3	RESERVED	R	2h	**Reserved** Always read back 2h
2:0	DEV_ID[2:0]	R	xh	**Channel ID** These bits indicates number of channels. 000 = 4-channel ADS1294 or ADS1294R 001 = 6-channel ADS1296 or ADS1296R 010 = 8-channel ADS1298 or ADS1298R 011 = Reserved 111 = Reserved

9.6.2 CONFIG1: Configuration Register 1 (address = 01h) (reset = 06h)

This register is configured with DAISY-EN_ bit, clock, and data rate.

7	6	5	4	3	2	1	0
HR	$\overline{\text{DAISY\_EN}}$	CLK_EN	0	0	DR[2:0]		
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-6h		

Table 9.6.3 Configuration Register 1 Field Description

Bit	Field	Type	Reset	Description
7	HR	R/W	0h	**High-resolution or low-power mode** This bit determines whether the device runs in low-power or high-resolution mode. 0 = LP mode 1 = HR mode
6	$\overline{\text{DAISY\_EN}}$	R/W	0h	**Daisy-chain or multiple readback mode** This bit determines which mode is enabled. 0 = Daisy-chain mode 1 = Multiple readback mode
5	CLK_EN	R/W	0h	**CLK connection**(1) This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1. 0 = Oscillator clock output disabled 1 = Oscillator clock output enabled
4:3	RESERVED	R/W	0h	**Reserved** Always write 0h
2:0	DR[2:0]	R/W	6h	**Output data rate** For High-Resolution mode, $f_{MOD} = f_{CLK} / 4$. For low power mode, $f_{MOD} = f_{CLK} / 8$. These bits determine the output data rate of the device. 000: f_{MOD} / 16 (HR Mode: 32 kSPS, LP Mode: 16 kSPS) 001: f_{MOD} / 32 (HR Mode: 16 kSPS, LP Mode: 8 kSPS) 010: f_{MOD} / 64 (HR Mode: 8 kSPS, LP Mode: 4 kSPS) 011: f_{MOD} / 128 (HR Mode: 4 kSPS, LP Mode: 2 kSPS) 100: f_{MOD} / 256 (HR Mode: 2 kSPS, LP Mode: 1 kSPS) 101: f_{MOD} / 512 (HR Mode: 1 kSPS, LP Mode: 500 SPS) 110: f_{MOD} / 1024 (HR Mode: 500 SPS, LP Mode: 250 SPS) 111: Reserved (do not use)

(1) Driving external chips will consume additional power.

9.6.3 PROFIG2: Configuration Register 2 (Address=02h) (Reset=40h)

This register is mainly used to configure the generation of test signals.

Figure 9.6.3 PROFIG2: Configuration Register 2

7	6	5	4	3	2	1	0
0	0	WCT_CHOP	INT_TEST	0	TEST_AMP	TEST_FREQ[1:0]	
R/W-1h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.4 Configuration Register 2 Field Description

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	1h	**Reserved** Always write 0h
5	WCT_CHOP	R/W	0h	**WCT chopping scheme** This bit determines whether the chopping frequency of WCT amplifiers is variable or fixed. 0 = Chopping frequency varies, see Table 7 1 = Chopping frequency constant at f_{MOD} / 16
4	INT_TEST	R/W	0h	**TEST source** This bit determines the source for the test signal. 0 = Test signals are driven externally 1 = Test signals are generated internally
3	RESERVED	R/W	0h	**Reserved** Always write 0h
2	TEST_AMP	R/W	0h	**Test signal amplitude** These bits determine the calibration signal amplitude. 0 = 1 × –(VREFP – VREFN) / 2400 V 1 = 2 × –(VREFP – VREFN) / 2400 V
1:0	TEST_FREQ[1:0]	R/W	0h	**Test signal frequency** These bits determine the calibration signal frequency. 00 = Pulsed at f_{CLK} / 2^{21} 01 = Pulsed at f_{CLK} / 2^{20} 10 = Not used 11 = At dc

9.6.4 PROFIG3: Configuration Register 3 (Address=03h) (Reset=40h)

This register is configured for internal or external reference and BIAS operations.

Figure 9.6.4 PROFIG3: Configuration Register 3

7	6	5	4	3	2	1	0
$\overline{\text{PD\_REFBUF}}$	1	VREF_4V	RLD_MEAS	RLDREF_INT	$\overline{\text{PD\_RLD}}$	RLD_LOFF_SENS	RLD_STAT
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.5 Configuration Register 3 Field Description

Bit	Field	Type	Reset	Description
7	$\overline{\text{PD\_REFBUF}}$	R/W	0h	**Power-down reference buffer** This bit determines the power-down reference buffer state. 0 = Power-down internal reference buffer 1 = Enable internal reference buffer
6	RESERVED	R/W	1h	**Reserved** Always write 1h
5	VREF_4V	R/W	0h	**Reference voltage** This bit determines the reference voltage, VREFP. 0 = VREFP is set to 2.4 V 1 = VREFP is set to 4 V (use only with a 5-V analog supply)
4	RLD_MEAS	R/W	0h	**RLD measurement** This bit enables RLD measurement. The RLD signal may be measured with any channel. 0 = Open 1 = RLD_IN signal is routed to the channel that has the MUX_Setting *010* (V_{REF})
3	RLDREF_INT	R/W	0h	**RLDREF signal** This bit determines the RLDREF signal source. 0 = RLDREF signal fed externally 1 = RLDREF signal (AVDD – AVSS) / 2 generated internally
2	$\overline{\text{PD\_RLD}}$	R/W	0h	**RLD buffer power** This bit determines the RLD buffer power state. 0 = RLD buffer is powered down 1 = RLD buffer is enabled
1	RLD_LOFF_SENS	R/W	0h	**RLD sense function** This bit enables the RLD sense function. 0 = RLD sense is disabled 1 = RLD sense is enabled
0	RLD_STAT	R	0h	**RLD lead-off status** This bit determines the RLD status. 0 = RLD is connected 1 = RLD is not connected

9.65 LOFF: Lead-Off Control Register (address = 04h) (reset = 00h)

The lead-off control register configures the lead-off detection operation.

Figure 9.6.5 LOFF: Lead-Off Control Register

7	6	5	4	3	2	1	0
COMP_TH2[2:0]			VLEAD_OFF_EN	ILEAD_OFF[1:0]		FLEAD_OFF[1:0]	
R/W-0h			R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.6. Lead-Off Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	COMP_TH[2:0]	R/W	0h	**Lead-off comparator threshold** Comparator positive side 000 = 95% 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% Comparator negative side 000 = 5% 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
4	VLEAD_OFF_EN	R/W	0h	**Lead-off detection mode** This bit determines the lead-off detection mode. 0 = Current source mode lead-off 1 = pullup or pulldown resistor mode lead-off
3:2	ILEAD_OFF[1:0]	R/W	0h	**Lead-off current magnitude** These bits determine the magnitude of current for the current lead-off mode. 00 = 6 nA 01 = 12 nA 10 = 18 nA 11 = 24 nA
1:0	FLEAD_OFF[1:0]	R/W	0h	**Lead-off frequency** These bits determine the frequency of lead-off detect for each channel. 00 = When any bits of the LOFF_SENSP or LOFF_SENSN registers are turned on, make sure that FLEAD[1:0] are either set to 01 or 11 01 = AC lead-off detection at f_{DR} / 4 10 = Do not use 11 = DC lead-off detection turned on

9.6.6 CHnSET: Individual Channel Settings (n = 1 to 8) (address = 05h to 0Ch) (reset = 00h)

The CH[1:8]SET control register configures the power mode, PGA gain, and multiplexer settings channels. See the Input Multiplexer section for details. CH[2:8]SET are similar to CH1SET,corresponding to the respective channels.

Figure 9.6.6. CHnSET: Individual Channel Settings Register

7	6	5	4	3	2	1	0
PD*n*	GAIN*n*[2:0]			0	MUX*n*[2:0]		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.7. Individual Channel Settings (n = 1 to 8) Field Descriptions

Bit	Field	Type	Reset	Description
7	PD*n*	R/W	0h	**Power-down** This bit determines the channel power mode for the corresponding channel. 0 = Normal operation 1 = Channel power-down. When powering down a channel, TI recommends that the channel be set to input short by setting the appropriate MUXn[2:0] = 001 of the CHnSET register.
6:4	GAIN*n*[2:0]	R/W	0h	**PGA gain** These bits determine the PGA gain setting. 000 = 6 001 = 1 010 = 2 011 = 3 100 = 4 101 = 8 110 = 12
3	RESERVED	R/W	0h	**Reserved** Always write 0h
2:0	MUX*n*[2:0]	R/W	0h	**Channel input** These bits determine the channel input selection. 000 = Normal electrode input 001 = Input shorted (for offset or noise measurements) 010 = Used in conjunction with RLD_MEAS bit for RLD measurements. See the *Right Leg Drive (RLD) DC Bias Circuit* subsection of the *ECG-Specific Functions* section for more details. 011 = MVDD for supply measurement 100 = Temperature sensor 101 = Test signal 110 = RLD_DRP (positive electrode is the driver) 111 = RLD_DRN (negative electrode is the driver)

9.6.7 RLD_SENSP: RLD Positive Signal Derivation Register (address = 0Dh) (reset = 00h)

This register controls the selection of the positive signals from each channel for right leg drive (RLD) derivation.

Figure 9.6.7. RLD_SENSP: RLD Positive Signal Derivation Register

7	6	5	4	3	2	1	0
RLD8P	RLD7P	RLD6P	RLD5P	RLD4P	RLD3P	RLD2P	RLD1P
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.8. RLD Positive Signal Derivation Field Descriptions

Bit	Field	Type	Reset	Description
7	RLD8P	R/W	0h	**IN8P to RLD** Route channel 8 positive signal into RLD derivation 0: Disabled 1: Enabled
6	RLD7P	R/W	0h	**IN7P to RLD** Route channel 7 positive signal into RLD derivation 0: Disabled 1: Enabled
5	RLD6P	R/W	0h	**IN6P to RLD** Route channel 6 positive signal into RLD derivation 0: Disabled 1: Enabled
4	RLD5P	R/W	0h	**IN5P to RLD** Route channel 5 positive signal into RLD derivation 0: Disabled 1: Enabled
3	RLD4P	R/W	0h	**IN4P to RLD** Route channel 4 positive signal into RLD derivation 0: Disabled 1: Enabled
2	RLD3P	R/W	0h	**IN3P to RLD** Route channel 3 positive signal into RLD derivation 0: Disabled 1: Enabled
1	RLD2P	R/W	0h	**IN2P to RLD** Route channel 2 positive signal into RLD channel 0: Disabled 1: Enabled
0	RLD1P	R/W	0h	**IN1P to RLD** Route channel 1 positive signal into RLD channel 0: Disabled 1: Enabled

9.6.8 RLD_SENSN: RLD Negative Signal Derivation Register (address = 0Eh) (reset = 00h)

This register controls the selection of the negative signals from each channel for right leg drive derivation. See the Right Leg Drive (RLD) DC Bias Circuit section for details.

Figure 9.6.8. RLD_SENSN: RLD Negative Signal Derivation Register

7	6	5	4	3	2	1	0
RLD8N	RLD7N	RLD6N	RLD5N	RLD4N	RLD3N	RLD2N	RLD1N
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.9. RLD Negative Signal Derivation Field Descriptions

Bit	Field	Type	Reset	Description
7	RLD8N	R/W	0h	**IN8N to RLD** Route channel 8 negative signal into RLD derivation 0: Disabled 1: Enabled
6	RLD7N	R/W	0h	**IN7N to RLD** Route channel 7 negative signal into RLD derivation 0: Disabled 1: Enabled
5	RLD6N	R/W	0h	**IN6N to RLD** Route channel 6 negative signal into RLD derivation 0: Disabled 1: Enabled
4	RLD5N	R/W	0h	**IN5N to RLD** Route channel 5 negative signal into RLD derivation 0: Disabled 1: Enabled
3	RLD4N	R/W	0h	**IN4N to RLD** Route channel 4 negative signal into RLD derivation 0: Disabled 1: Enabled
2	RLD3N	R/W	0h	**IN3N to RLD** Route channel 3 negative signal into RLD derivation 0: Disabled 1: Enabled
1	RLD2N	R/W	0h	**IN2N to RLD** Route channel 2 negative signal into RLD derivation 0: Disabled 1: Enabled
0	RLD1N	R/W	0h	**IN1N to RLD** Route channel 1 negative signal into RLD derivation 0: Disabled 1: Enabled

9.6.9 LOFF_SENSP: Positive Signal Lead-Off Detection Register (address = 0Fh) (reset = 00h)

This register selects the positive side from each channel for lead-off detection. See the Lead-Off Detection section for details. The LOFF_STATP register bits are only valid if the corresponding LOFF_SENSP bits are set to 1.

Figure 9.6.9. LOFF_SENSP: Positive Signal Lead-Off Detection Register

7	6	5	4	3	2	1	0
LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.10. Positive Signal Lead-Off Detection Field Descriptions

Bit	Field	Type	Reset	Description
7	LOFF8P	R/W	0h	**IN8P lead off** Enable lead-off detection on IN8P 0: Disabled 1: Enabled
6	LOFF7P	R/W	0h	**IN7P lead off** Enable lead-off detection on IN7P 0: Disabled 1: Enabled
5	LOFF6P	R/W	0h	**IN6P lead off** Enable lead-off detection on IN6P 0: Disabled 1: Enabled
4	LOFF5P	R/W	0h	**IN5P lead off** Enable lead-off detection on IN5P 0: Disabled 1: Enabled
3	LOFF4P	R/W	0h	**IN4P lead off** Enable lead-off detection on IN4P 0: Disabled 1: Enabled
2	LOFF3P	R/W	0h	**IN3P lead off** Enable lead-off detection on IN3P 0: Disabled 1: Enabled
1	LOFF2P	R/W	0h	**IN2P lead off** Enable lead-off detection on IN2P 0: Disabled 1: Enabled
0	LOFF1P	R/W	0h	**IN1P lead off** Enable lead-off detection on IN1P 0: Disabled 1: Enabled

9.6.10 LOFF_SENSN: Negative Signal Lead-Off Detection Register (address = 10h) (reset = 00h)

This register selects the negative side from each channel for lead-off detection. See the Lead-Off Detection section for details. The LOFF_STATN register bits are only valid if the corresponding LOFF_SENSN bits are set to 1.

Figure 9.6.10. LOFF_SENSN: Negative Signal Lead-Off Detection Register

7	6	5	4	3	2	1	0
LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.11. Negative Signal Lead-Off Detection Field Descriptions

Bit	Field	Type	Reset	Description
7	LOFF8N	R/W	0h	**IN8N lead off** Enable lead-off detection on IN8N 0: Disabled 1: Enabled
6	LOFF7N	R/W	0h	**IN7N lead off** Enable lead-off detection on IN7N 0: Disabled 1: Enabled
5	LOFF6N	R/W	0h	**IN6N lead off** Enable lead-off detection on IN6N 0: Disabled 1: Enabled
4	LOFF5N	R/W	0h	**IN5N lead off** Enable lead-off detection on IN5N 0: Disabled 1: Enabled
3	LOFF4N	R/W	0h	**IN4N lead off** Enable lead-off detectionn on IN4N 0: Disabled 1: Enabled
2	LOFF3N	R/W	0h	**IN3N lead off** Enable lead-off detectionion on IN3N 0: Disabled 1: Enabled
1	LOFF2N	R/W	0h	**IN2N lead off** Enable lead-off detectionction on IN2N 0: Disabled 1: Enabled
0	LOFF1N	R/W	0h	**IN1N lead off** Enable lead-off detectionction on IN1N 0: Disabled 1: Enabled

9.6.11 LOFF_FLIP: Lead-Off Flip Register (address = 11h) (reset = 00h)

This register controls the direction of the current used for lead-off derivation. See the Lead-Off Detection section for details.

Figure 9.6.11. LOFF_FLIP: Lead-Off Flip Register

7	6	5	4	3	2	1	0
LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.12. Lead-Off Flip Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOFF_FLIP8	R/W	0h	**Channel 8 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 8 for lead-off derivation. 0: No Flip: IN8P is pulled to AVDD and IN8N pulled to AVSS 1: Flipped: IN8P is pulled to AVSS and IN8N pulled to AVDD
6	LOFF_FLIP7	R/W	0h	**Channel 7 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 7 for lead-off derivation. 0: No Flip: IN7P is pulled to AVDD and IN7N pulled to AVSS 1: Flipped: IN7P is pulled to AVSS and IN7N pulled to AVDD
5	LOFF_FLIP6	R/W	0h	**Channel 6 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 6 for lead-off derivation. 0: No Flip: IN6P is pulled to AVDD and IN6N pulled to AVSS 1: Flipped: IN6P is pulled to AVSS and IN6N pulled to AVDD
4	LOFF_FLIP5	R/W	0h	**Channel 5 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 5 for lead-off derivation. 0: No Flip: IN5P is pulled to AVDD and IN5N pulled to AVSS 1: Flipped: IN5P is pulled to AVSS and IN5N pulled to AVDD
3	LOFF_FLIP4	R/W	0h	**Channel 4 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 4 for lead-off derivation. 0: No Flip: IN4P is pulled to AVDD and IN4N pulled to AVSS 1: Flipped: IN4P is pulled to AVSS and IN4N pulled to AVDD
2	LOFF_FLIP3	R/W	0h	**Channel 3 LOFF polarity flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 3 for lead-off derivation. 0: No Flip: IN3P is pulled to AVDD and IN3N pulled to AVSS 1: Flipped: IN3P is pulled to AVSS and IN3N pulled to AVDD
1	LOFF_FLIP2	R/W	0h	**Channel 2 LOFF Polarity Flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 2 for lead-off derivation. 0: No Flip: IN2P is pulled to AVDD and IN2N pulled to AVSS 1: Flipped: IN2P is pulled to AVSS and IN2N pulled to AVDD
0	LOFF_FLIP1	R/W	0h	**Channel 1 LOFF Polarity Flip** Flip the pullup/pulldown polarity of the current source or resistor on channel 1 for lead-off derivation. 0: No Flip: IN1P is pulled to AVDD and IN1N pulled to AVSS 1: Flipped: IN1P is pulled to AVSS and IN1N pulled to AVDD

9.6.12 LOFF_STATP: Lead-Off Positive Signal Status Register (address = 12h) (reset = 00h)

This register stores the status of whether the positive electrode on each channel is on or off. See the Lead-Off Detection section for details. Ignore the LOFF_STATP values if the corresponding LOFF_SENSP bits are not set to 1. When the LOFF_SENSEP bits are 0, the LOFF_STATP bits should be ignored.

Figure 9.6.12. LOFF_STATP: Lead-Off Positive Signal Status Register (Read-Only)

7	6	5	4	3	2	1	0
IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.13. Lead-Off Positive Signal Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8P_OFF	R	0h	**Channel 8 positive channel lead-off status** Status of whether IN8P electrode is on or off 0: Electrode is on 1: Electrode is off
6	IN7P_OFF	R	0h	**Channel 7 positive channel lead-off status** Status of whether IN7P electrode is on or off 0: Electrode is on 1: Electrode is off
5	IN6P_OFF	R	0h	**Channel 6 positive channel lead-off status** Status of whether IN6P electrode is on or off 0: Electrode is on 1: Electrode is off
4	IN5P_OFF	R	0h	**Channel 5 positive channel lead-off status** Status of whether IN5P electrode is on or off 0: Electrode is on 1: Electrode is off
3	IN4P_OFF	R	0h	**Channel 4 positive channel lead-off status** Status of whether IN4P electrode is on or off 0: Electrode is on 1: Electrode is off
2	IN3P_OFF	R	0h	**Channel 3 positive channel lead-off status** Status of whether IN3P electrode is on or off 0: Electrode is on 1: Electrode is off
1	IN2P_OFF	R	0h	**Channel 2 positive channel lead-off status** Status of whether IN2P electrode is on or off 0: Electrode is on 1: Electrode is off
0	IN1P_OFF	R	0h	**Channel 1 positive channel lead-off status** Status of whether IN1P electrode is on or off 0: Electrode is on 1: Electrode is off

9.6.1.13 LOFF_STATN: Lead-Off Negative Signal Status Register (address = 13h) (reset = 00h)

This register stores the status of whether the negative electrode on each channel is on or off. See the Lead-Off Detection section for details. Ignore the LOFF_STATN values if the corresponding LOFF_SENSN bits are not set to 1. When the LOFF_SENSEN bits are 0, the LOFF_STATP bits should be ignored.

Figure 9.6.13. LOFF_STATN: Lead-Off Negative Signal Status Register (Read-Only)

7	6	5	4	3	2	1	0
IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.14. Lead-Off Negative Signal Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8N_OFF	R	0h	**Channel 8 negative channel lead-off status** Status of whether IN8N electrode is on or off 0: Electrode is on 1: Electrode is off
6	IN7N_OFF	R	0h	**Channel 7 negative channel lead-off status** Status of whether IN7N electrode is on or off 0: Electrode is on 1: Electrode is off
5	IN6N_OFF	R	0h	**Channel 6 negative channel lead-off status** Status of whether IN6N electrode is on or off 0: Electrode is on 1: Electrode is off
4	IN5N_OFF	R	0h	**Channel 5 negative channel lead-off status** Status of whether IN5N electrode is on or off 0: Electrode is on 1: Electrode is off
3	IN4N_OFF	R	0h	**Channel 4 negative channel lead-off status** Status of whether IN4N electrode is on or off 0: Electrode is on 1: Electrode is off
2	IN3N_OFF	R	0h	**Channel 3 negative channel lead-off status** Status of whether IN3N electrode is on or off 0: Electrode is on 1: Electrode is off
1	IN2N_OFF	R	0h	**Channel 2 negative channel lead-off status** Status of whether IN2N electrode is on or off 0: Electrode is on 1: Electrode is off
0	IN1N_OFF	R	0h	**Channel 1 negative channel lead-off status** Status of whether IN1N electrode is on or off 0: Electrode is on 1: Electrode is off

9.6.1.14 GPIO: General-Purpose I/O Register (address = 14h) (reset = 0Fh)

The general-purpose I/O register controls the action of the three GPIO pins. When RESP_CTRL[1:0] is in mode 01 and 11, the GPIO2, GPIO3, and GPIO4 pins are not available for use.

Figure 9.6.14. GPIO: General-Purpose I/O Register

7	6	5	4	3	2	1	0
GPIOD[4:1]				GPIOC[4:1]			
R/W-0h				R/W-Fh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.15. General-Purpose I/O Field Descriptions

Bit	Field	Type	Reset	Description
7:4	GPIOD[4:1]	R/W	0h	**GPIO data** These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect. GPIO is not available in certain respiration modes.
3:0	GPIOC[4:1]	R/W	Fh	**GPIO control (corresponding GPIOD)** These bits determine if the corresponding GPIOD pin is an input or output. 0 = Output 1 = Input

9.6.15 PACE: Pace Detect Register (address = 15h) (reset = 00h)

This register provides the pace controls that configure the channel signal used to feed the external pace detect circuitry. See the Pace Detect section for details.

Figure 9.6.15. PACE: Pace Detect Register

7	6	5	4	3	2	1	0
0	0	0	PACEE[1:0]		PACEO[1:0]		$\overline{\text{PD\_PACE}}$
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.16. (For example, CONTROL_REVISION Register) Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0h	**Reserved** Always write 0h
4:3	PACEE[1:0]	R/W	0h	**Pace even channels** These bits control the selection of the even number channels available on TEST_PACE_OUT1. Only one channel may be selected at any time. 00 = Channel 2 01 = Channel 4 10 = Channel 6 11 = Channel 8
2:1	PACEO[1:0]	R/W	0h	**Pace odd channels** These bits control the selection of the odd number channels available on TEST_PACE_OUT2. Only one channel may be selected at any time. 00 = Channel 1 01 = Channel 3 10 = Channel 5 11 = Channel 7
0	$\overline{\text{PD\_PACE}}$	R/W	0h	**Pace detect buffer** This bit is used to enable/disable the pace detect buffer. 0 = Pace detect buffer turned off 1 = Pace detect buffer turned on

9.6.16 RESP: Respiration Control Register (address = 16h) (reset = 00h)

This register provides the controls for the respiration circuitry; see the Respiration section for details.

Figure 9.6.16. RESP: Respiration Control Register

7	6	5	4	3	2	1	0
RESP_ DEMOD_EN1	RESP_MOD_ EN1	1	RESP_PH[2:0]			RESP_CTRL[1:0]	
R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.17. Respiration Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	hold	R/W	0h	hold

9.6.17 CONFIG4: Configuration Register 4 (address = 17h) (reset = 00h)

Figure 9.6.17. CONFIG4: Configuration Register 4

7	6	5	4	3	2	1	0
RESP_FREQ[2:0]			0	SINGLE_SHOT	WCT_TO_RLD	PD_LOFF_COMP	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.18. Configuration Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESP_FREQ[2:0]	R/W	0h	**Respiration modulation frequency** These bits control the respiration control frequency when RESP_CTRL[1:0] = 10 or RESP_CTRL[1:0] = 10(1). 000 = 64 kHz modulation clock 001 = 32 kHz modulation clock 010 = 16kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 011 = 8kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 100 = 4kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 101 = 2kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 110 = 1kHz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. 111 = 500Hz square wave on GPIO3 and GPIO04. Output on GPIO4 is 180 degree out of phase with GPIO3. Modes 000 and 001 are modulation frequencies in internal and external respiration modes. In internal respiration mode, the control signals appear at the RESP_MODP and RESP_MODN terminals. All other bit settings generate square waves as described above on GPIO4 and GPIO3.
4	RESERVED	R/W	0h	**Reserved** Always write 0h
3	SINGLE_SHOT	R/W	0h	**Single-shot conversion** This bit sets the conversion mode. 0 = Continuous conversion mode 1 = Single-shot mode
2	WCT_TO_RLD	R/W	0h	**Connects the WCT to the RLD** This bit connects WCT to RLD. 0 = WCT to RLD connection off 1 = WCT to RLD connection on
1	PD_LOFF_COMP	R/W	0h	**Lead-off comparator power-down** This bit powers down the lead-off comparators. 0 = Lead-off comparators disabled 1 = Lead-off comparators enabled
0	RESERVED	R/W	0h	**Reserved** Always write 0h

9.6.18 WCT1: Wilson Central Terminal and Augmented Lead Control Register (address = 18h) (reset = 00h)

The WCT1 control register configures the device WCT circuit channel selection and the augmented leads.

Figure 9.6.18. WCT1: Wilson Central Terminal and Augmented Lead Control Register

7	6	5	4	3	2	1	0
aVF_CH6	aVL_CH5	aVR_CH7	aVR_CH4	PD_WCTA	WCTA[2:0]		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.19. Wilson Central Terminal and Augmented Lead Control Field Descriptions

Bit	Field	Type	Reset	Description
7	aVF_CH6	R/W	0h	**Enable (WCTA + WCTB)/2 to the negative input of channel 6** 0 = Disabled 1 = Enabled
6	aVL_CH5	R/W	0h	**Enable (WCTA + WCTC)/2 to the negative input of channel 5** 0 = Disabled 1 = Enabled
5	aVR_CH7	R/W	0h	**Enable (WCTB + WCTC)/2 to the negative input of channel 7** 0 = Disabled 1 = Enabled
4	aVR_CH4	R/W	0h	**Enable (WCTB + WCTC)/2 to the negative input of channel 4** 0 = Disabled 1 = Enabled
3	$\overline{\text{PD\_WCTA}}$	R/W	0h	**Power-down WCTA** 0 = Powered down 1 = Powered on
2:0	WCTA[2:0]	R/W	0h	**WCT Amplifier A channel selection, typically connected to RA electrode** These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTA amplifier 001 = Channel 1 negative input connected to WCTA amplifier 010 = Channel 2 positive input connected to WCTA amplifier 011 = Channel 2 negative input connected to WCTA amplifier 100 = Channel 3 positive input connected to WCTA amplifier 101 = Channel 3 negative input connected to WCTA amplifier 110 = Channel 4 positive input connected to WCTA amplifier 111 = Channel 4 negative input connected to WCTA amplifier

9.6.19 WCT2: Wilson Central Terminal Control Register (address = 18h) (reset = 00h)

The WCT2 configuration register configures the device WCT circuit channel selection.

Figure 9.6.19. WCT2: Wilson Central Terminal Control Register

7	6	5	4	3	2	1	0
$\overline{\text{PD\_WCTC}}$	$\overline{\text{PD\_WCTB}}$	WCTB[2:0]			WCTC[2:0]		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9.6.20. Wilson Central Terminal Control Field Descriptions

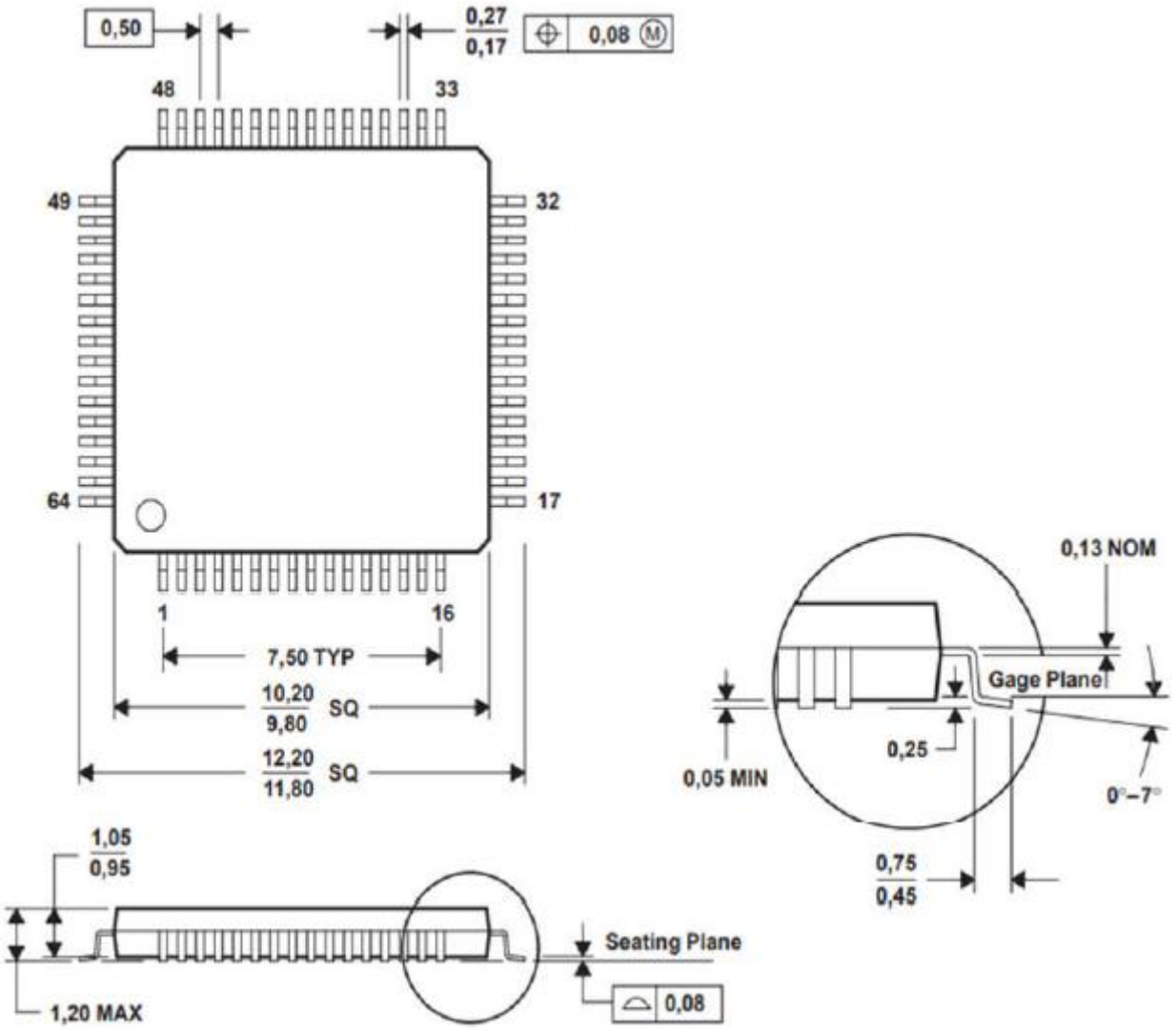
Bit	Field	Type	Reset	Description
7	PD_WCTC	R/W	0h	**Power-down WCTC** 0 = Powered down 1 = Powered on
6	PD_WCTB	R/W	0h	**Power-down WCTB** 0 = Powered down 1 = Powered on
5:3	WCTB[2:0]	R/W	0h	**WCT amplifier B channel selection, typically connected to LA electrode.** These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTB amplifier 001 = Channel 1 negative input connected to WCTB amplifier 010 = Channel 2 positive input connected to WCTB amplifier 011 = Channel 2 negative input connected to WCTB amplifier 100 = Channel 3 positive input connected to WCTB amplifier 101 = Channel 3 negative input connected to WCTB amplifier 110 = Channel 4 positive input connected to WCTB amplifier 111 = Channel 4 negative input connected to WCTB amplifier
2:0	WCTC[2:0]	R/W	0h	**WCT amplifier C channel selection, typically connected to LL electrode.** These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTC amplifier 001 = Channel 1 negative input connected to WCTC amplifier 010 = Channel 2 positive input connected to WCTC amplifier 011 = Channel 2 negative input connected to WCTC amplifier 100 = Channel 3 positive input connected to WCTC amplifier 101 = Channel 3 negative input connected to WCTC amplifier 110 = Channel 4 positive input connected to WCTC amplifier 111 = Channel 4 negative input connected to WCTC amplifier

Applications matters

NOTE :

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Outline Dimensions



Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PAKEAGE OPTION	MAKING INFORMATION
CBM24AD98Q		-40℃~85℃	LQFP-64	Tray，960	
CBM24AD98Q		-40℃~85℃	LQFP-64	Tray，960	
CBM24AD98Q		-40℃~85℃	LQFP-64	Tray，960	