Features

- 1.8 V supply operation
- Low power: 164 mW per channel at 125 MSPS with scalable power options
- SNR = 76.5 dBFS @ 70 MHz (2.0Vp-p input span)
- SNR = 77.5 dBFS @ 70 MHz (2.6Vp-p Input span)
- SFDR = 90 dBc (to Nyquist)
- DNL = ±0.7 LSB (typical);INL = ±3.5 LSB (typical)
- Serial LVDS (ANSI-644, default) and low power, reduced signal option (similar to IEEE 1596.3)
- 650 MHz full power analog bandwidth
- 2V p-p input voltage range (supports up to 2.6 V p-p)
- Serial port control

Application

- Medical ultrasound and MRI
- High speed imaging
- Quadrature radio receivers
- Diversity radio receivers
- Test equipment

Description

The CBM96AD53 is a quad, 16-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.
The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications. The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual channel power-down is supported and typically consumes less than 2 mW when all channels are disabled. The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable output clock and data alignment and digital test pattern generation. The

available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The CBM96AD53 is available in a RoHS-compliant, 48-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C.

Catalog

Pin Configurations

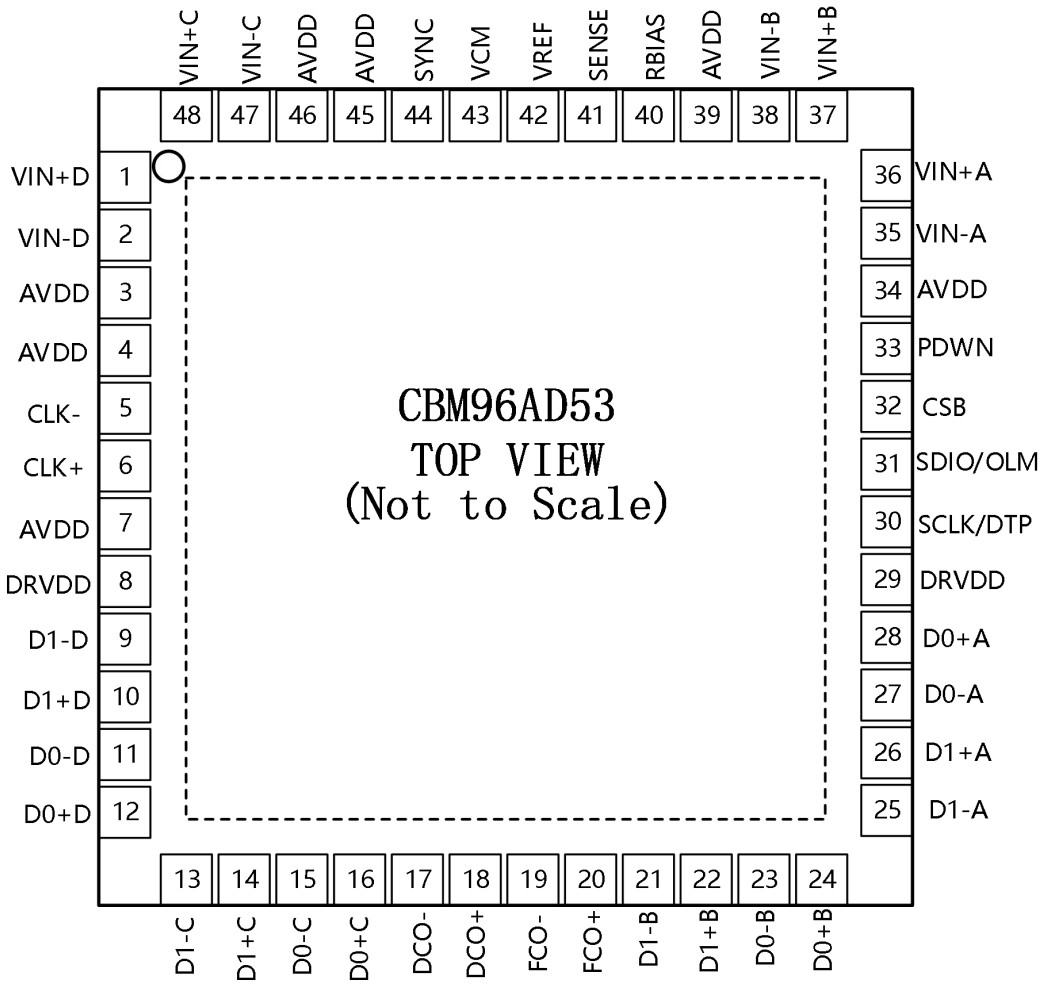

Figure 1. Pin Configuration

Pin Description

Pin Number	Symbol	Pin Description
0	AGND,Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
1	VIN+D	ADC D Analog Input True.
2	VIN−D	ADC D Analog Input Complement.
3,4,7,34,39, 45,46	AVDD	1.8 V Analog Supply Pins.
5,6	CLK−, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
8,29	DRVDD	Digital Output Driver Supply.
9,10	FCO−, FCO+	Frame Clock Outputs.
11,12	D0−D, D0+D	Channel D Digital Outputs, (disabled in One-Lane Mode1).
13,14	D1−C, D1+C	Channel C Digital Outputs, (Channel D Digital Outputs in One-Lane Mode1).
15,16	D0−C, D0+C	Channel C Digital Outputs.
17,18	DCO−, DCO+	Data Clock Outputs.
19,20	FCO−, FCO+	Frame Clock Outputs.
21,22	D1−B, D1+B	Channel B Digital Outputs.
23,24	D0−B, D0+B	Channel B Digital Outputs, (Channel A Digital Outputs in One-Lane Mode1).
25,26	D1−A, D1+A	Channel A Digital Outputs, (Disabled in One-Lane Mode1).
27,28	D0−A, D0+A	Channel A Digital Outputs, (Disabled in One-Lane Mode1).
30	SCLK/DTP	SPI Clock Input/Digital Test Pattern.
31	SDIO/OLM	SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode.
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up.
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device.

		PDWN low = run device, normal operation.
35	VIN-A	ADC A Analog Input Complement.
36	VIN+A	ADC A Analog Input True.
37	VIN+B	ADC B Analog Input True.
38	VIN−B	ADC B Analog Input Complement.
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
41	SENSE	Reference Mode Selection.
42	VREF	Voltage Reference Input and Output.
43	VCM	Analog Output at Midsupply Voltage. Sets the common mode of the analog inputs, external to the ADC, as shown in Figure 15 and Figure 16.
44	SYNC	Digital Input. SYNC input to clock divider.
47	VIN−C	ADC C Analog Input Complement.
48	VIN+C	ADC C Analog Input True.

Block Diagram and Timing Characteristics

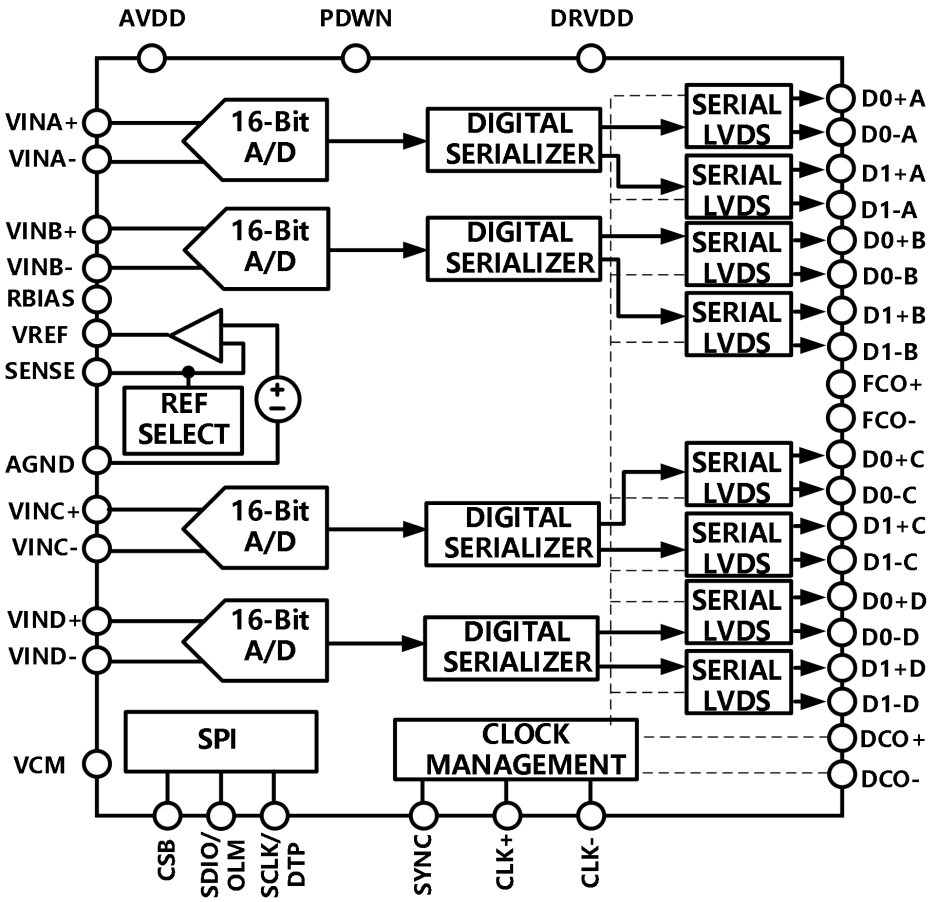

Figure 2. Block Diagram

Timing Diagrams

Refer to the Memory Map Register Descriptions section and Table 12 for SPI register settings.

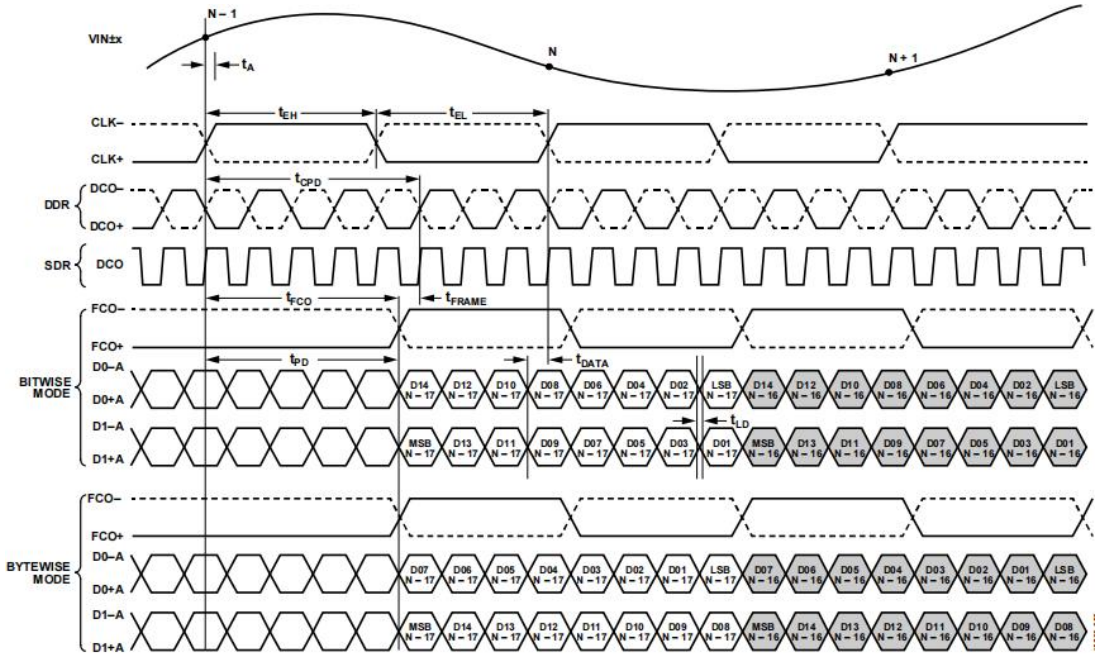

Figure 3. 16-Bit DDR/SDR, Two-Lane, 1× Frame Mode (Default)

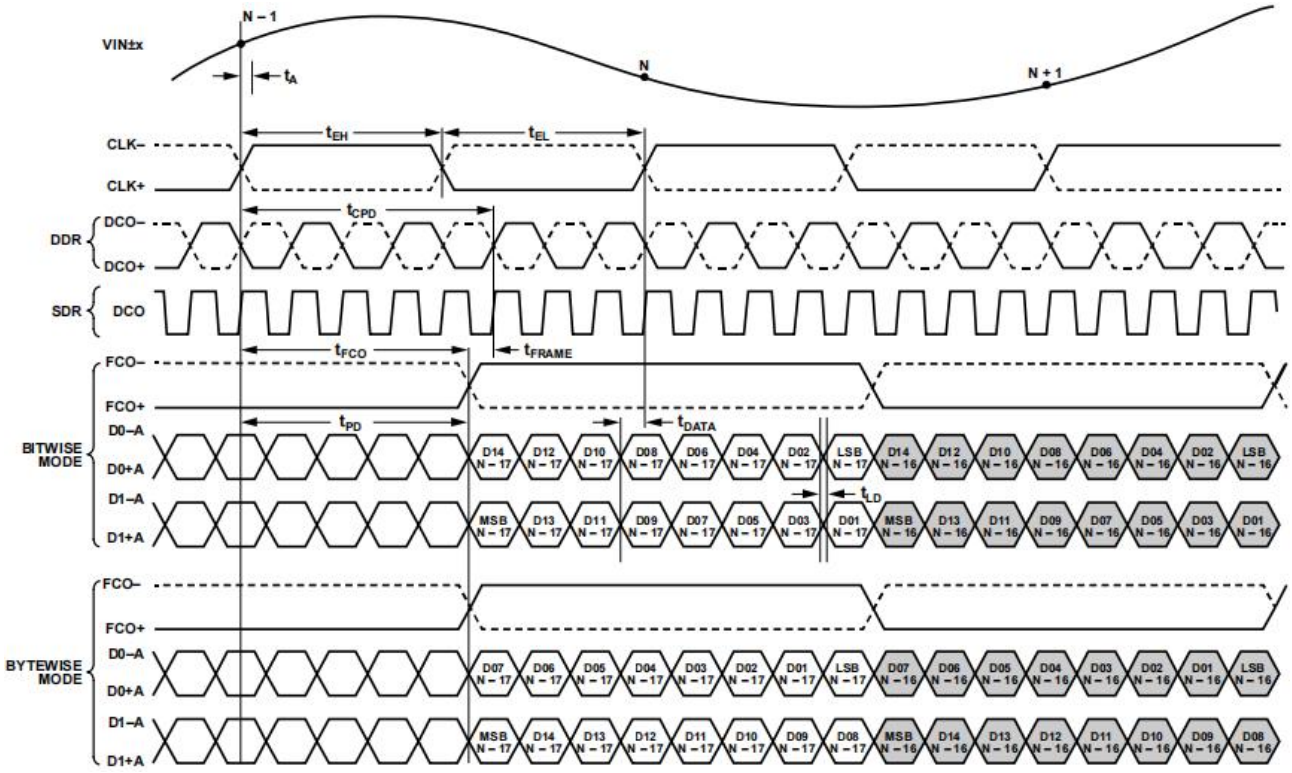

Figure 4. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode

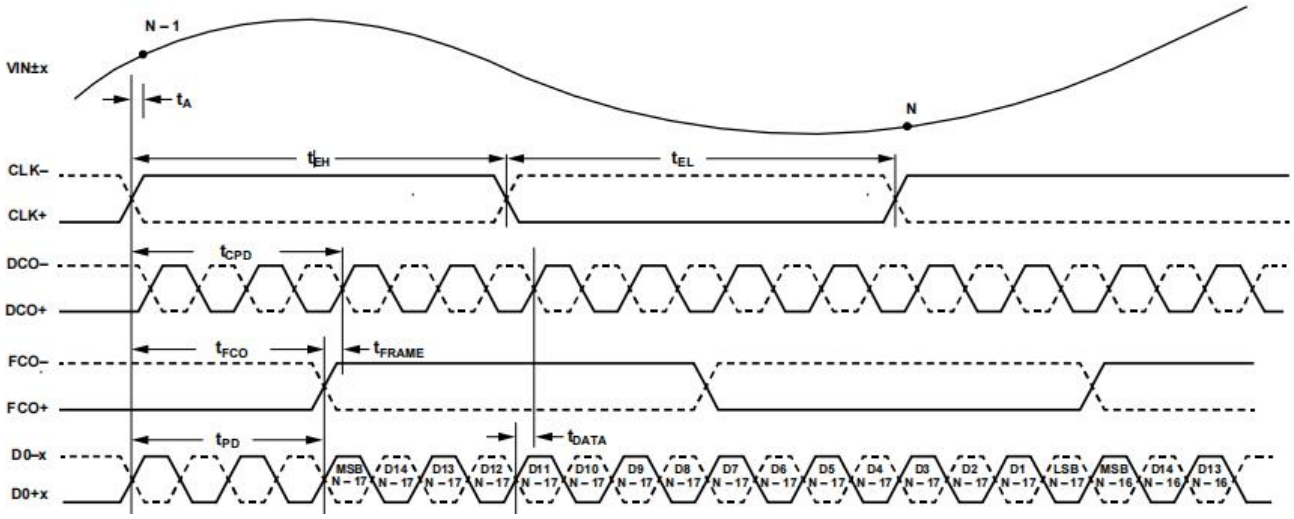

Figure 5. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode

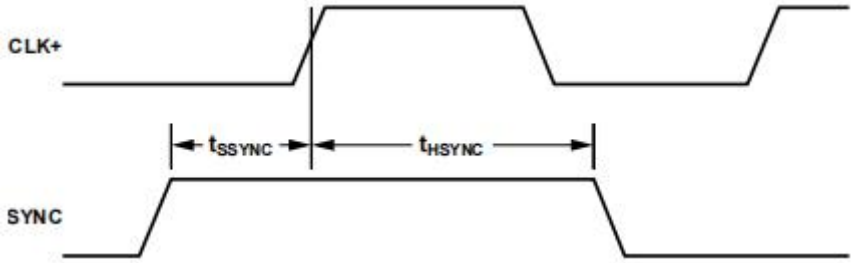

Figure 6. SYNC Input Timing Requirements

Absolute Maximum Ratings (1)

- AVDD,DRVDD to AGND : −0.3 V to +2.0 V
- Digital Outputs (D0±x, D1±x, DCO+, DCO−, FCO+, FCO−) to AGND : −0.3 V to +2.0 V
- CLK+, CLK−,VIN+x, VIN−x,SCLK/DTP, SDIO/OLM, CSB,SYNC to AGND : −0.3 V to +2.0 V
- PDWN,RBIAS, VCM,VREF, SENSE to AGND : −0.3 V to +2.0 V
- Operating Temperature Rangee (Ambient, VREF = 1.0 V) : −40°C to +85°C
- Operating Temperature Rangee (Ambient, VREF = 1.3 V) : 0°C to +85°C
- Lead Temperature (Soldering, 10 sec) : 300°C
- Storage Temperature Range : −65°C to +150°C
- Junction Temperature : 150°C

DC Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.0 V, DCS off, unless otherwise noted.

Table 1.

Parameter	Temperature	CBM96AD53			Unit
		Min	Typ	Max	
Resolution	--		16		Bit
Accuracy					
No Missing Codes	Full	--	--	--	--
Offset Error	Full	-0.49	-0.3	0.17	%FSR
Offset Matching	Full	-0.14	+0.2	0.39	%FSR
Gain Error	Full	-12.3	-5	2.37	%FSR
Gain Matching	Full	1.0	1.1	5.8	%FSR
Differential Nonlinearity (DNL)	Full	-0.77	--	0.95	LSB
	25℃	--	±0.7	--	LSB
Integral Nonlinearity (INL)	Full	-7.26	--	--	LSB
	25℃	--	±3.5	--	LSB
TEMPERATURE DRIFT					
Offset Error	Full	--	3.5	--	ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1.0 V Mode)	Full	0.98	1.0	1.02	V
Load Regulation at 1.0 mA (V_{REF} = 1.0 V)	Full	--	2	--	mV
Input Resistance	25℃	--	7.5	--	KΩ
INPUT-REFERRED NOISE					
V_{REF} = 1.0 V	25℃	--	2.7	--	LSB rms
ANALOG INPUTS					
Differential Input	Full	--	2	--	Vp-p

Voltage (V_{REF} = 1.0 V)					
Common-Mode Voltage	Full	--	0.9	--	V
Common-Mode Range	25℃	0.5	--	1.3	V
Differential Input Resistance	25℃	--	2.6	--	kΩ
Differential Input Capacitance	25℃	--	7	--	pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD2}	Full	--	305	330	mA
I_{DRVDD} (ANSI-644 Mode)2	Full	--	60	64	mA
I_{DRVDD} (Reduced Range Mode)2	25℃	--	45	--	mA
TOTAL POWER CONSUMPTION					
DC Input	Full	--	607	649	mW
Sine Wave Input (Four Channels Including Output Drivers, ANSI-644 Mode)	Full	--	657	708	mW
Sine Wave Input (Four ChannelsIncluding Output Drivers, Reduced Range Mode)	25℃	--	630	--	mW
Power-Down	25℃	--	2	--	mW
Standby3	Full	--	356	392	mW

AVDD = 1.8 V, DRVDD = 1.8 V, 2.6 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.3 V; 0°C to 85°C, DCS off, unless otherwise noted.

Table 2.

Parameter	Temperature	CBM96AD53			Unit
		Min	Typ	Max	
Resolution	-		16		Bit
Accuracy					
No Missing Codes	25℃	--	--	--	--
Offset Error	25℃	--	-0.3	--	%FSR
Offset Matching	25℃	--	+0.2	--	%FSR
Gain Error	25℃	--	-5	--	%FSR
Gain Matching	25℃	--	1.1	--	%FSR
Differential Nonlinearity (DNL)	25℃	--	±0.8	--	LSB
Integral Nonlinearity (INL)	25℃	--	±5.0	--	LSB
TEMPERATURE DRIFT					
Offset Error	25℃	--	3.5	--	ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1.0 V Mode)	25℃	--	1.3	--	V
Load Regulation at 1.0 mA (V_{REF} = 1.0 V)	25℃	--	6.5	--	mV
Input Resistance	25℃	--	7.5	--	KΩ
INPUT-REFERRED NOISE					
VREF = 1.3 V	25℃	--	2.1	--	LSB rms
ANALOG INPUTS					
Differential Input Voltage (V_{REF} = 1.3V)	25℃	--	2.6	--	Vp-p
Common-Mode Voltage	25℃	--	0.9	--	V
Common-Mode	25℃	0.6	--	1.3	V

Range					
Differential Input Resistance	25℃	--	2.6	--	kΩ
Differential Input Capacitance	25℃	--	7	--	pF
POWER SUPPLY					
AVDD	25℃	--	1.8	--	V
DRVDD	25℃	--	1.8	--	V
I_{AVDD2}	25℃	--	314	--	mA
I_{DRVDD} (ANSI-644 Mode)2	25℃	--	60	--	mA
I_{DRVDD} (Reduced Range Mode)2	25℃	--	45	--	mA
TOTAL POWER CONSUMPTION					
DC Input	25℃	--	614	--	mW
Sine Wave Input (Four Channels Including Output Drivers, ANSI-644 Mode)	25℃	--	673	--	mW
Sine Wave Input (Four ChannelsIncluding Output Drivers, Reduced Range Mode)	25℃	--	646	--	mW
Power-Down	25℃	--	2	--	mW
Standby3	25℃	--	371	--	mW

AC Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.0 V, DCS off, unless otherwise noted.

Table 3.

Parameter	Temperature	CBM96AD53			Unit
		Min	Typ	Max	
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25℃	--	78	--	dBFS
f_{IN} = 15 MHz	25℃	--	77.8	--	dBFS
f_{IN} = 70 MHz	Full	75.5	76.5	--	dBFS
f_{IN} = 128 MHz	25℃	--	73.9	--	dBFS
f_{IN} = 200 MHz	25℃	--	71.5	--	dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25℃	--	78	--	dBFS
f_{IN} = 15 MHz	25℃	--	77.7	--	dBFS
f_{IN} = 70 MHz	Full	74.6	76.1	--	dBFS
f_{IN} = 128 MHz	25℃	--	73.6	--	dBFS
f_{IN} = 200 MHz	25℃	--	70.3	--	dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25℃	--	12.7	--	Bits
f_{IN} = 15 MHz	25℃	--	12.6	--	Bits
f_{IN} = 70 MHz	Full	12.1	12.3	--	Bits
f_{IN} = 128 MHz	25℃	--	11.9	--	Bits
f_{IN} = 200 MHz	25℃	--	11.4	--	Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25℃	--	96	--	dBc
f_{IN} = 15 MHz	25℃	--	93	--	dBc
f_{IN} = 70 MHz	Full	78	89	--	dBc
f_{IN} = 128 MHz	25℃	--	87	--	dBc

f_{IN} = 200 MHz	25°C	--	77	--	dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25°C	--	-98	--	dBc
f_{IN} = 15 MHz	25°C	--	-93	--	dBc
f_{IN} = 70 MHz	Full	--	-89	-78	dBc
f_{IN} = 128 MHz	25°C	--	-87	--	dBc
f_{IN} = 200 MHz	25°C	--	-77	--	dBc
WORST OTHER HARMONIC OR SPUR					
f_{IN} = 9.7 MHz	25°C	--	-96	--	dBc
f_{IN} = 15 MHz	25°C	--	-98	--	dBc
f_{IN} = 70 MHz	Full	--	-94	-85	dBc
f_{IN} = 128 MHz	25°C	--	-89	--	dBc
f_{IN} = 200 MHz	25°C	--	-83	--	dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz	25°C	--	-90	--	dBc
CROSSTALK2	25°C	--	-91	--	dB
CROSSTALK (OVERRANGE CONDITION)3	25°C	--	-87	--	dB
POWER SUPPLY REJECTION RATIO (PSRR)4					
AVDD	25°C	--	31	--	dB
DRVDD	25°C	--	79	--	dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C	--	650	--	MHz

AVDD = 1.8 V, DRVDD = 1.8 V, 2.6 V p-p full-scale differential input at −1.0 dBFS; V_{REF} = 1.3 V; 0°C to 85°C, DCS off, unless otherwise noted.

Table 4.

Parameter	Temperature	CBM96AD53			Unit
		Min	Typ	Max	
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C	--	80	--	dBFS
f_{IN} = 15 MHz	25°C	--	79.4	--	dBFS
f_{IN} = 70 MHz	25°C	75.5	77.5	--	dBFS

f_{IN} = 128 MHz	25℃	--	74.4	--	dBFS
f_{IN} = 200 MHz	25℃	--	71.7	--	dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)					
f_{IN} = 9.7 MHz	25℃	--	79.8	--	dBFS
f_{IN} = 15 MHz	25℃	--	79.2	--	dBFS
f_{IN} = 70 MHz	25℃	--	76.1	--	dBFS
f_{IN} = 128 MHz	25℃	--	74	--	dBFS
f_{IN} = 200 MHz	25℃	--	69.9	--	dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25℃	--	13	--	Bits
f_{IN} = 15 MHz	25℃	--	12.9	--	Bits
f_{IN} = 70 MHz	25℃	12.1	12.3	--	Bits
f_{IN} = 128 MHz	25℃	--	12	--	Bits
f_{IN} = 200 MHz	25℃	--	11.3	--	Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25℃	--	94	--	dBc
f_{IN} = 15 MHz	25℃	--	94	--	dBc
f_{IN} = 70 MHz	25℃	--	82	--	dBc
f_{IN} = 128 MHz	25℃	--	86	--	dBc
f_{IN} = 200 MHz	25℃	--	75	--	dBc
WORST HARMONIC (SECOND OR THIRD)					
f_{IN} = 9.7 MHz	25℃	--	-94	--	dBc
f_{IN} = 15 MHz	25℃	--	-94	--	dBc
f_{IN} = 70 MHz	25℃	--	-82	--	dBc
f_{IN} = 128 MHz	25℃	--	-87	--	dBc
f_{IN} = 200 MHz	25℃	--	-75	--	dBc
WORST OTHER HARMONIC OR SPUR					
f_{IN} = 9.7 MHz	25℃	--	-100	--	dBc
f_{IN} = 15 MHz	25℃	--	-99	--	dBc
f_{IN} = 70 MHz	25℃	--	-96	--	dBc
f_{IN} = 128 MHz	25℃	--	-86	--	dBc

f_{IN} = 200 MHz	25℃	--	-84	--	dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS					
fIN1 = 70.5 MHz, fIN2 = 72.5 MHz	25℃	--	-90	--	dBc
CROSSTALK2	25℃	--	91	--	dB
CROSSTALK (OVERRANGE CONDITION)3	25℃	--	87	--	dB
POWER SUPPLY REJECTION RATIO (PSRR)4					
AVDD	25℃	--	31	--	dB
DRVDD	25℃	--	79	--	dB
ANALOG INPUT BANDWIDTH, FULL POWER	25℃	--	650	--	MHz

Digital Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, unless otherwise noted.

Table 5.

Parameter	Temperature	CBM96AD53			Unit
		Min	Typ	Max	
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	--	--	CMOS/LVDS/LVPECL	--	--
Differential Input Voltage2	Full	0.2	--	3.6	Vp-p
Input Voltage Range	Full	AGND −0.2	--	AVDD + 0.2	V
Input Common-Mode Voltage	Full	--	0.9	--	V
Input Resistance (Differential)	25℃	--	15	--	kΩ
Input Capacitance	25℃	--	4	--	pF
LOGIC INPUTS (PDWN, SYNC, SCLK)					
Logic 1 Voltage	Full	1.2	--	AVDD + 0.2	V
Logic 0 Voltage	Full	0	--	0.8	V
Input Resistance	25℃	--	30	--	kΩ
Input Capacitance	25℃	--	2	--	pF
LOGIC INPUT (CSB)					

Logic 1 Voltage	Full	1.2	--	AVDD + 0.2	V
Logic 0 Voltage	Full	0	--	0.8	V
Input Resistance	25℃	--	26	--	kΩ
Input Capacitance	25℃	--	2	--	pF
LOGIC INPUT (SDIO)					
Logic 1 Voltage	Full	1.2	--	AVDD + 0.2	V
Logic 0 Voltage	Full	0	--	0.8	V
Input Resistance	25℃	--	26	--	kΩ
Input Capacitance	25℃	--	5	--	pF
LOGIC INPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full	--	1.79	--	V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	--	--	0.05	V
DIGITAL OUTPUTS (D0±x, D1±x), ANSI-644					
Logic Compliance	--	--	LVDS	--	--
Differential Output Voltage (V_{OD})	Full	±290	±345	±400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)	--	--	Twos complement	--	--

Switchings Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, unless otherwise noted.

Table 6.

Parameter	Temperature	CBM96AD53			Unit
		Min	Typ	Max	
CLOCK[3]					
Input Clock Rate	Full	20	--	1000	MHz
Conversion Rate[4]	Full	20	--	125	MSPS
Clock Pulse Width High (t_{EH})	Full	--	4.00	--	ns
Clock Pulse Width Low (t_{EL})	Full	--	4.00	--	ns
OUTPUT PARAMETERS[3]					
Propagation Delay (t_{PD})	Full	1.5	2.3	3.1	ns

Rise Time (t_R) (20% to 80%)	Full	--	300	--	ps
Fall Time (t_F) (20% to 80%)	Full	--	300	--	ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[5]	Full	--	t_{FCO} + (t_{SAMPLE}/16)	--	MHz
DCO to Data Delay (t_{DATA}) 5	Full	(t_{SAMPLE}/16) – 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	MSPS
DCO to FCO Delay (t_{FRAME}) 5	Full	(t_{SAMPLE}/16) – 300	(t_{SAMPLE}/16)	(t_{SAMPLE}/16) + 300	ns
Lane Delay (t_{LD})	Full	--	90	--	ns
Data to Data Skew ($t_{DATA-MAX}$ – $t_{DATA-MIN}$)	Full	20	±50	±200	MHz
Wake-Up Time (Standby)	25℃	--	250	--	MSPS
Wake-Up Time (Power-Down)6	25℃	--	375	--	ns
Pipeline Latency	Full	--	16	--	ns
APERTURE					
Aperture Delay (tA)	25℃	--	1	--	ns
Aperture Uncertainty (Jitter, t_J)	25℃	--	135	--	fs rms
Out-of-Range Recovery Time	25℃	--	1	--	Clock cycles

Timing Specifications

Table 7.

Parameter	Description	CBM96AD53			Unit
		Min	Typ	Max	
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	1.2	--	--	ns
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	-0.2	--	--	ns
SPI TIMING REQUIREMENTS					

t_{DS}	Setup time between the data and the rising edge of SCLK	2	--	--	ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2	--	--	ns
t_{CLK}	Period of the SCLK	40	--	--	ns
t_S	Setup time between CSB and SCLK	2	--	--	ns
t_H	Hold time between CSB and SCLK	2	--	--	ns
t_{HIGH}	SCLK pulse width high	10	--	--	ns
t_{LOW}	SCLK pulse width low	10	--	--	ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	--	--	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	--	--	ns

Memory Map Register Table

The CBM96AD53 uses a 3-wire interface and 16-bit addressing and, therefore, Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1. When Bit 5 in Register 0x00 is set high, the SPI enters a soft reset, where all of the user registers revert to their default values and Bit 2 is automatically cleared.

Table 8.

Address	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
0x00	SPI port configuration (global)	0 = SDO active	LSB first	Soft reset	1 = 16-bit address	1 = 16-bit address	Soft reset	LSB first	0 = SDO active	0x18	R/W
0x01	Chip ID (global)	8-bit Chip ID [7:0],0xB5 = quad, 16-bit, 125 MSPS serial LVDS								0xB5	R
0x02	Chip grade(global)	Open	Speed grade ID[6:4] 110 = 125 MSPS			Open	Open	Open	Open		R
Device Index and Transfer Registers											
0x04	Device index	Open	Open			Data Channel D	Data Channel C	Data Channel B	Data Channel A	0x0F	R/W
0x05	Device index	Open	Open	Clock Channel DCO	Clock Channel FCO	Data Channel D	Data Channel C	Data Channel B	Data Channel A	0x3F	R/W
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Initiate override	0x00	W
Global ADC Function Registers											
0x08	Power modes (local)	Open	Open	External power-down pin function 0 = full power-down 1 = standby	Open	Open	Open	Power mode 00 = chip run 01 = full power-down 10 = standby 11 = reset		0x00	R/W

0x09	Clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer: 1=off 0=on	0x01	R/W
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio[2:0] 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	R/W
0x0D	Test mode (local except for PN sequence resets)	User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once (affects user input test mode only, Bits[3:0] = 1000)		Reset PN long gen	Reset PN short gen	Output test mode[3:0] (local) 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/zero word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency				0x00	R/W
0x10	Offset adjust(local)	8-bit device offset adjustment [7:0] (local) Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	R/W
0x14	Output mode	Open	LVDS-ANSI/ LVDS-IEEE option 0 = LVDS-ANSI 1 = LVDS-IEEE reduced range link (global) see Table 9	Open	Open	Open	Output invert (local)	1	Output format 0 = offset binary 1 = twos compl e-men t (global)	0x03	R/W

0x15	Output adjust	Open	Open	Output driver termination[1:0] 00 = none 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω	Open	Open	Open	Output drive 0 = 1× drive 1 = 2× drive	0x00	R/W
0x16	Output phase	Open	Input clock phase adjust[6:4] (value is number of input clock cycles of phase delay) see Table 10		Output clock phase adjust[3:0] (0000 through 1011) see Table 11				0x03	R/W
0x18	V_{REF}	Open		Open	Open	Open	V_{REF} adjustment digital scheme[2:0] 000 = 1.0 V p-p (1.3 V p-p) 001 = 1.14 V p-p (1.48 V p-p) 010 = 1.33 V p-p (1.73 V p-p) 011 = 1.6 V p-p (2.08 V p-p) 100 = 2.0 V p-p (2.6 V p-p)			0x04	R/W
0x19	USER_PATT1_ LSB (global)	B7	B6	B5	B4	B3	B2	B2	B0	0x00	R
0x1A	USER_PATT1_ MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	R
0x1B	USER_PATT2_ LSB (global)	B7	B6	B5	B4	B3	B2	B2	B0	0x00	R
0x1C	USER_PATT2_ MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	R
0x21	Serial output data control (global)	LVDS output LSB first	SDR/DDR one-lane/two-lane, bitwise/bytewise[6:4] 000 = SDR two-lane, bitwise 001 = SDR two-lane, bytewise 010 = DDR two-lane, bitwise 011 = DDR two-lane, bytewise 100 = DDR one-lane, wordwise			Open	Select 2× frame	Serial output number of bits 00 = 16 bits		0x30	Serial stream control. Default causes MSB first and the native bit stream.
0x22	Serial channel status (local)	Open	Open	Open	Open	Open	Open	Channel output reset	Channel power-down	0x00	Used to power down individual sections of a converter.

0x100	Sample rate override	Open	Sample rate override enable	0	0	Open	Sample rate 000 = 20 MSPS 001 = 40 MSPS 010 = 50 MSPS 011 = 65 MSPS 100 = 80 MSPS 101 = 105 MSPS 110 = 125 MSPS			0x00	Sample rate override (requires transfer register, 0xFF).
0x101	User Input/Output Control 2	Open	Open	Open	Open	Open	Open	Open	SDIO pull-down	0x00	Disables SDIO pull-down.
0x102	User Input/Output Control 3	Open	Open	Open	Open	VCM power-down	Open	Open	Open	0x00	VCM control.
0x109	Sync	Open	Open	Open	Open	Open	Open	Sync next only	Enable sync	0x00	

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0xFF, Interfacing to High Speed ADCs via SPI.

Device Index (Register 0x04, Register 0x05)

There are certain features in the map that can be set independently for each channel, whereas other features apply globally to all channels (depending on context) regardless of which are selected. The first four bits in Register 0x04 and Register 0x05 are used to select which individual data channels are affected. The output clock channels can be selected in Register 0x05 as well. A smaller subset of the independent feature list can be applied to those devices. Register 0x04 Bits[3:0] must be set to the same value as

Register 0x05 Bits[3:0]

Transfer (Register 0xFF)

All registers except Register 0x100 are updated the moment they are written. Setting Bit 0 of this transfer register high initializes the settings in the sample rate override register (Address 0x100).

Power Modes (Register 0x08)

Bits[7:6]—Open

Bit 5—External Power-Down Pin Function

If set, the external PDWN pin initiates standby mode. If cleared, the external PDWN pin initiates power-down mode.

Bits[4:2]—Open

Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), all ADC channels are active. In power-down mode (Bits[1:0] = 01), the digital datapath clocks are disabled while the digital datapath is reset. Outputs are disabled. In standby mode (Bits[1:0] = 10), the digital datapath clocks and the outputs are disabled. During a digital reset (Bits[1:0] = 11), all the digital datapath clocks and the outputs (where applicable) on the chip are reset, except the SPI port. Note that the SPI is always left under control of the user; that is, it is never automatically disabled or in reset (except by power-on reset).

Clock (Register 0x09)

Bits[7:1]—Open

Bit 0—Duty Cycle Stabilize

The default state is Bit 0 = 1, duty cycle stabilizer off. Note that, when the part is not in SPI mode, the duty cycle stabilizer is on. Refer to the Configuration Without the SPI section for more information.

Enhancement Control (Register 0x0C)

Bits[7:3]—Open

Bit 2—Chop Mode

For applications that are sensitive to offset voltages and other low frequency noise, such as homodyne or direct conversion receivers, chopping in the first stage of the CBM96AD53 is a feature

that can be enabled by setting Bit 2. In the frequency domain, chopping translates offsets and other low frequency noise to fCLK/2 where it can be filtered.

Bits[1:0]—Open

Output Mode (Register 0x14)

Bit 7—Open

Bit 6—LVDS-ANSI/LVDS-IEEE Option

Setting this bit chooses LVDS-IEEE (reduced range) option. The default setting is LVDS-ANSI. As described in Table 9, when LVDS-ANSI or LVDS-IEEE reduced range link is selected, the user can select the driver termination. The driver current is automatically selected to give the proper output swing.

Table 9. LVDS-ANSI/LVDS-IEEE Options

Output Mode, Bit 6	Output Mode	Output Driver Termination	Output Driver Current
0	LVDS-ANSI	User selectable	Automatically selected to give proper swing
1	LVDS-IEEE reduced range link	User selectable	Automatically selected to give proper swing

Bits[5:3]—Open

Bit 2—Output Invert

Setting this bit inverts the output bit stream.

Bit 1—1

Bit 0—Output Format

By default, this bit is set to send the data output in twos complement format. Resetting this bit changes the output mode to offset binary.

Output Adjust (Register 0x15)

Bits[7:6]—Open

Bits[5:4]—Output Driver Termination

These bits allow the user to select the internal termination resistor.

Bits[3:1]—Open

Bit 0—Output Drive

Bit 0 of the output adjust register controls the drive strength on the LVDS driver of the FCO and DCO outputs only. The default values set the drive to 1× while the drive can be increased to 2× by setting the appropriate channel bit in Register 0x05 and then setting Bit 0. These features cannot be used with the output driver termination select. The termination selection takes precedence over the 2× driver strength on FCO and DCO when both the output driver termination and output drive are selected.

Output Phase (Register 0x16)

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Register 0x16 Bits[6:4] determine at which phase of the external clock the sampling occurs. This is applicable only when the clock divider is used. It is prohibited to select a value for Bits[6:4] that is greater than the value of Bits[2:0], Register 0x0B.

Table 10. Input Clock Phase Adjust Options

Input Clock Phase Adjust, Bits[6:4]	Number of Input Clock Cycles of Phase Delay
000 (Default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Bits[3:0]—Output Clock Phase Adjust

Table 11. Output Clock Phase Adjust Options

Output Clock (DCO), Phase Adjust, Bits[3:0]	DCO Phase Adjustment (Degrees Relative to D0±x/D1±x Edge)
0000	0
0001	60
0010	120
0011	180
0100	240
0101	300
0110	360
0111	420
1000	480
1001	540
1010	600
1011	660

Table 12. SPI Register Options

Register 0x21 Contents	**Serialization Options Selected**			**DCO Multiplier**	**Timing Diagram**
	Serial Output Number of Bits (SONB)	**Frame Mode**	**Serial Data Mode**		
0x30	16-bit	1x	DDR two-lane, bytewise	4 × f_S	Figure 3 (default setting)
0x20	16-bit	1x	DDR two-lane, bitwise	4 × f_S	Figure 3
0x10	16-bit	1x	SDR two-lane, bytewise	8 × f_S	Figure 3
0x00	16-bit	1x	SDR two-lane, bitwise	8 × f_S	Figure 3
0x34	16-bit	2x	DDR two-lane, bytewise	4 × f_S	Figure 3
0x24	16-bit	2x	DDR two-lane, bitwise	4 × f_S	Figure 3
0x14	16-bit	2x	SDR two-lane,	8 × f_S	Figure 3

			bytewise		
0x04	16-bit	2x	SDR two-lane, bitwise	8 × f_S	Figure 3
0x40	16-bit	1x	DDR one-lane, wordwise	8 × f_S	Figure 3

Serial Output Data Control (Register 0x21)

The serial output data control register is used to program the CBM96AD53 in various output data modes depending upon the data capture solution. Table 12 describes the various serialization

options available in the CBM96AD53 .

Sample Rate Override (Register 0x100)

This register is designed to allow the user to downgrade the device (that is, establish lower power) for applications that do not require a full sample rate. Settings in this register are not initialized until Bit 0 of the transfer register (Register 0xFF) is set to 1. This function does not affect the sample rate; it affects the maximum sample rate capability of the ADC, as well as the resolution.

User Input/Output Control 2 (Register 0x101)

Bits[7:1]—Open

Bit 0—SDIO Pull-Down

Bit 0 can be set to disable the internal 30 kΩ pull-down on the SDIO pin, which can be used to limit the loading when many devices are connected to the SPI bus.

User Input/Output Control 3 (Register 0x102)

Bits[7:4]—Open

Bit 3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an external reference.

Bits[2:0]—Open

Equivalent Circuits

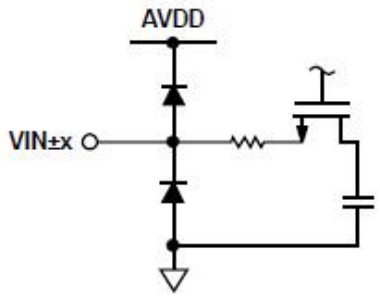

Figure 7. Equivalent Analog Input Circuit

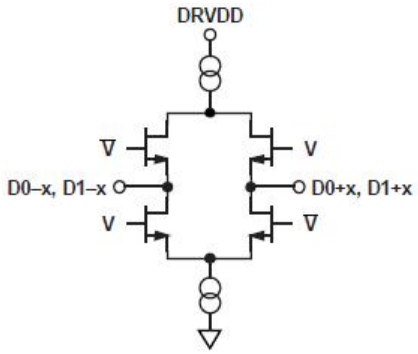

Figure 8. Equivalent Digital Output Circuit

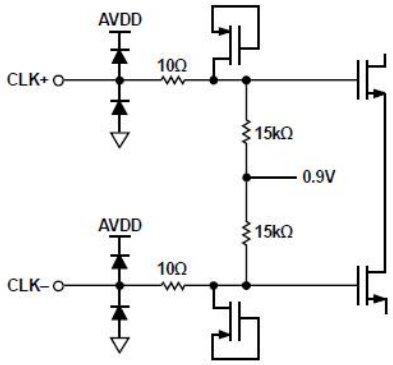

Figure 9. Equivalent Clock Input Circuit

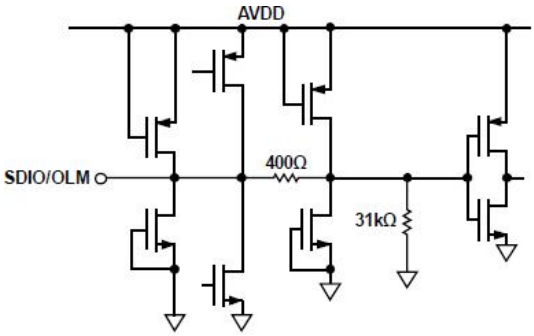

Figure 10. Equivalent SDIO/OLM Input Circuit

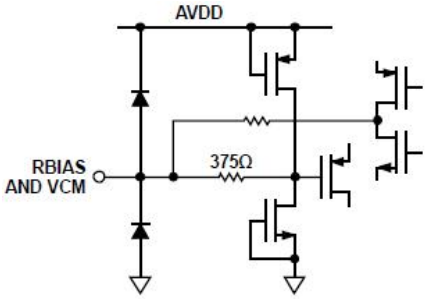

Figure 11. Equivalent RBIAS and VCM Circuit

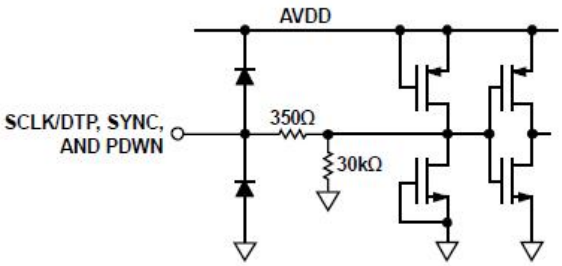

Figure 12. Equivalent SCLK/DTP, SYNC, and PDWN Input Circuit

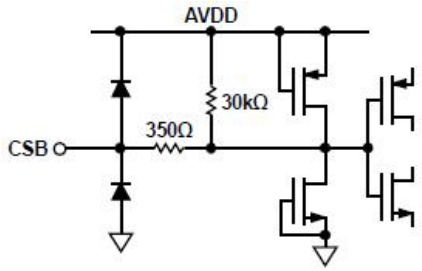

Figure 13. Equivalent CS Input Circuit

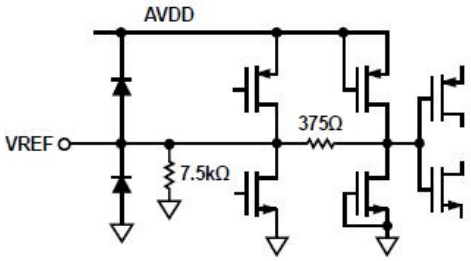

Figure 14. Equivalent VREF Circuit

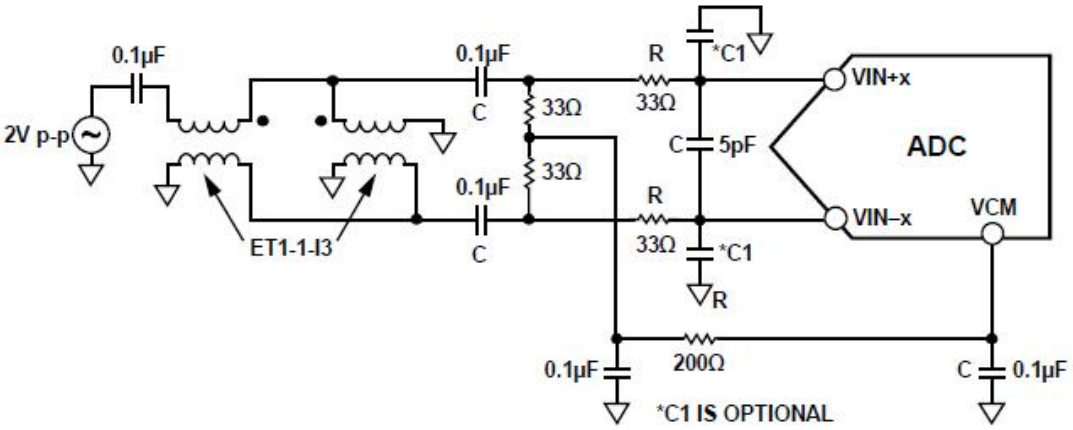

Figure 15. Differential Double Balun Input Configuration for Baseband Applications

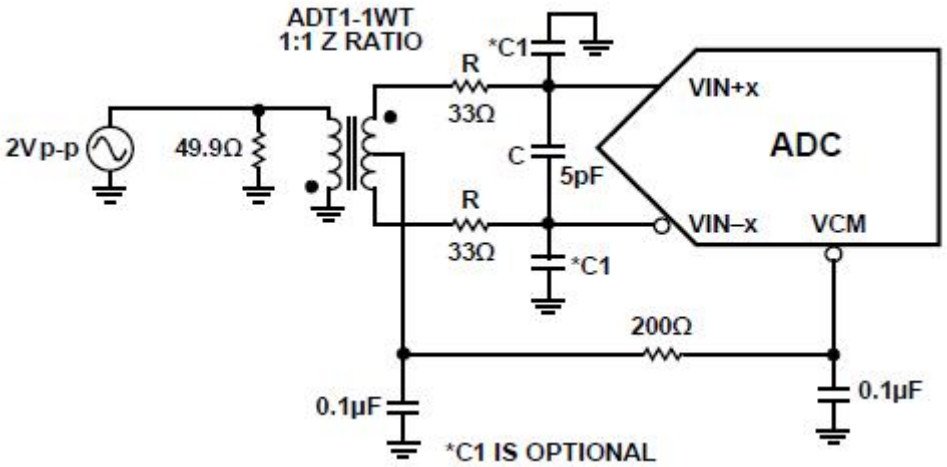

Figure 16. Differential Transformer-Coupled Configuration for Baseband Applications

Package Outline Dimensions

QFN-48

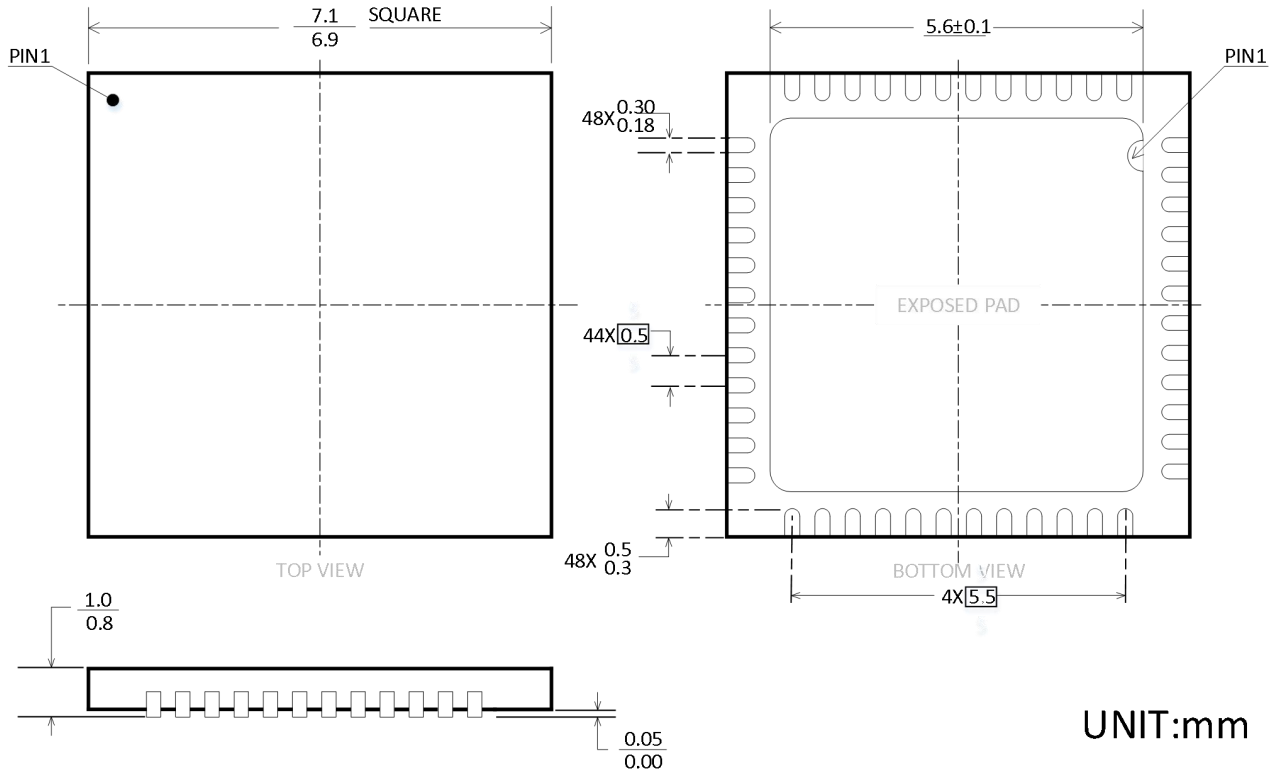

Figure 17. QFN-48 Packaging Dimensions

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PAKEAGE OPTION	MAKING INFORMATION
CBM96AD53		-40℃-85℃	QFN-48	Tray，250	