Features

- Low power: 800mW@125MSPS
- Power supply :1.8 V
- CMOS or LVDS output supply: 1.8V
- SNR=78dBFS (Fin=70MHz/Fs=125MSPS)
- Spurious free dynamic range (SFDR): 88dBc (Fin=70MHz/Fs=125MSPS)
- IF sampling frequencies to 300 MHz
- Integer 1-to-8 input clock divider
- small-signal input noise: −153dBm/Hz (200Ω Input impedance / Fin= 70MHz / Fs = 125MSPS)
- Programmable internal voltage reference
- Differential analog input range: 2Vp-p (maximum)
- Differential analog inputs bandwidth: 650MHz
- ADC clock duty cycle stabilizer
- 95 dB channel isolation/crosstalk
- Serial port (SPI) control
- User-configurable, built-in self-test (BIST) capability
- Energy-saving power-down modes

Applications

- Radar system
- Diversity radio system
- Multimode digital receivers (3G)
- GSM/EDGE/W-CDMA/LTE/CDMA2000 WiMAX/TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Broadband data applications
- Ultrasound equipment

Product Highlights

- On-chip dither option for improved SFDR performance with low power analog input.
- Proprietary differential input that maintains excellent SNR performance for input frequencies up to 300MHz.
- Operation from a single 1.8 V supply and a separate digital output driver supply accommodating 1.8 V CMOS or LVDS outputs.
- Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, test modes, and voltage reference mode.
- Pin compatibility with the AD9258/AD9268, allowing a simple migration from 16 bits to 14 bits.

General Description

The CBM16AD125 is a dual, 16-bit, 125 MSPS analog-to-digital converter (ADC). The CBM16AD125 is designed to support communications applications where high performance, combined with low cost, small size, and versatility, is desired.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth, differential sample-and-hold analog input amplifiers that support a variety of user-selectable input ranges. An integrated voltage reference eases design consideration. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC output data can be routed directly to the two external 16-bit output ports. These outputs can be set to either 1.8 V CMOS or LVDS.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface.

The CBM16AD125 is available in a 64-lead QFN and is specified over the industrial temperature range of −40°C to +85°C.

Catalog

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2024.8.20	Update product Outline Dimensions diagram, thickness parameter error	Error update	WW	LYL	
V1.1	2024.10.11	Increase the maximum rated parameter information	Routine updates	WW	LYL	

Functional Block Diagram

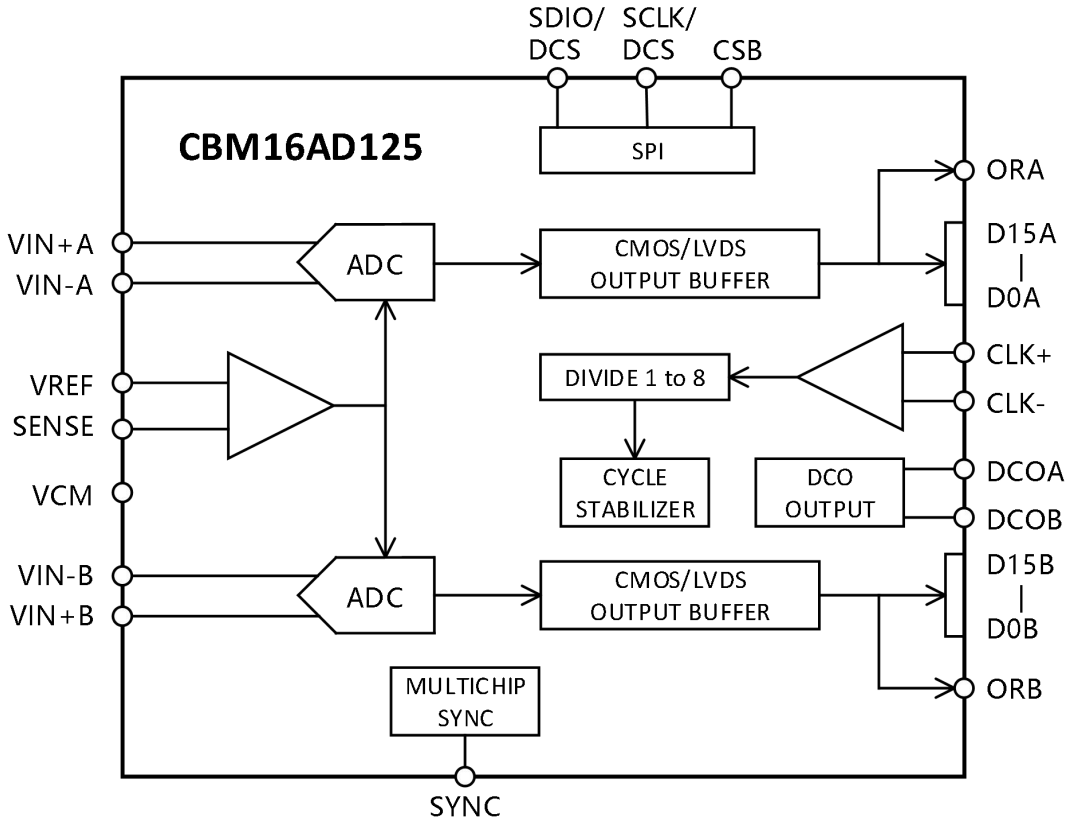


Figure 1. Functional Block Diagram

Specifications

ADC DC Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate=125MSPS, V_{IN} = −1.0dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ.	Max	Unit
RESOLUTION	Full		16		Bit
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±0.4	±0.7	% FSR
Gain Error	Full		±0.8	±2.5	% FSR
Differential Nonlinearity (DNL)[1]	Full	-1.2		+1.4	LSB
	25℃		±0.7		LSB
Integral Nonlinearity (INL)[1]	Full			±6.0	LSB
	25℃		±3.5		LSB
MATCHING CHARACTERISTIC					
Offset Error	Full		±0.2	±0.5	% FSR
Gain Error	Full		±0.3	±1.3	% FSR
INTERNAL VOLTAGE REFERENCE					
Output Voltage Error (1 V Mode)	Full		±5	±12	mV
Load Regulation (1.0mA)	Full		5		mV
INPUT REFERRED NOISE V_{REF} = 1.0 V	25℃		2.34		LSB rms
ANALOG INPUT					
Input Span,V_{REF} = 1.0 V	Full		2		V p-p
Input Capacitance[2]	Full		8		pF
Input Common-Mode Voltage	Full		0.9		V
Reference Input Resistance	Full		7		kΩ
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V

Supply Current					
IAVDD[1]	Full		370		mA
IDRVDD[1] (1.8 V CMOS)	Full		52		mA
IDRVDD[1](1.8 V LVDS)	Full		98		mA
POWER CONSUMPTION					
DC Input	Full		745	780	mW
Sine Wave Input[1] (1.8 V CMOS)	Full		795		mW
Sine Wave Input[1] (1.8 V LVDS)	Full		875		mW
Standby Power[3]	Full		49		mW
Power-Down Power	Full	0.5	2.7		mW

1.Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

2.Input capacitance refers to the effective capacitance between one differential input pin and AGND.

3.Standby power is measured with a dc input and with the CLK pins inactive (set to AVDD or AGND).

ADC AC Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate=125MSPS, V_{IN} = −1.0dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 2.

Parameter	Temp	Min	Typ.	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 30 MHz	25℃		77.9		dBFs
f_{IN} = 70 MHz	25℃		77.0		dBFs
	Full	74.7			dBc
f_{IN} = 140 MHz	25℃		75.6		dBFs
f_{IN} = 200 MHz	25℃		73.1		dBFs
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)					
f_{IN} = 30 MHz	25℃		77.7		dBFs
f_{IN} = 70 MHz	25℃		76.3		dBFs
f_{IN} = 140 MHz	25℃		73.8		dBFs
f_{IN} = 200 MHz	25℃		72.5		dBFs
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 30 MHz	25℃		12.6		Bit
f_{IN} = 70 MHz	25℃		12.4		Bit
f_{IN} = 140 MHz	25℃		12.0		Bit
f_{IN} = 200 MHz	25℃		11.8		Bit
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25℃		-86.5		dBc
f_{IN} = 70 MHz	25℃		-85.2		dBc
	Full	80.0			dBc
f_{IN} = 140 MHz	25℃		-80.1		dBc
f_{IN} = 200 MHz	25℃		-78.9		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25℃		86.5		dBc
f_{IN} = 70 MHz	25℃		85.2		dBc
	Full	80.0			dBc
f_{IN} = 140 MHz	25℃		80.1		dBc

f_{IN} = 200 MHz	25℃		78.9		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
Without Dither (AIN@ −23dBFS)					
f_{IN} = 30 MHz	25℃		92		dBFS
f_{IN} = 70 MHz	25℃		88		dBFS
f_{IN} = 140 MHz	25℃		96		dBFS
f_{IN} = 200 MHz	25℃		97		dBFS
With On-Chip Dither (AIN @ −23dBFS)					
f_{IN} = 30 MHz	25℃		104		dBFS
f_{IN} = 70 MHz	25℃		103		dBFS
f_{IN} = 140 MHz	25℃		105		dBFS
f_{IN} = 200 MHz	25℃		102		dBFS
Crosstalk	25℃		-95		dBc
Analog Input Bandwidth	25℃		650		MHz

Crosstalk measurement conditions：Crosstalk is measured at 100 MHz with −1dBFS on one channel and no input on the alternate channel.

Digital Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate=125MSPS, V_{IN} = −1.0dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	Min	Typ.	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.3	V
High Level Input Current	Full	-100		+100	μA
Low Level Input Current	Full	-120		+120	μA
Input Capacitance	Full		6.5		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					

Logic Compliance	Full		CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	-100		+100	μA
Low Level Input Current	Full	-120		+120	μA
Input Capacitance	Full		2		pF
Input Resistance	Full	12	16	20	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.2		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	-10		10	μA
Low Level Input Current	Full	10		100	μA
Input Resistance	Full		20		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS) [2]					
High Level Input Voltage	Full	1.2		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN=1.8 V)	Full	-10		-100	μA
Low Level Input Current	Full	-10		10	μA
Input Resistance	Full		25		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
CMOS Mode (DRVDD=1.8V)					
High Level Output Voltage					
I_{OH}=50μA	Full	1.79			V
I_{OH}=0.5mA	Full	1.75			V
Low Level Output Voltage					
I_{OL}=1.6mA	Full			0.2	V
I_{OL}=50μA	Full			0.05	V
LVDS Mode (DRVDD=1.8V)					

Differential Output Voltage (V_{OD}), ANSI Mode	Full	280	330	380	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	160	200	230	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

1．Pull up.。　　2．Pull down.

Switching Specifications

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate=125MSPS, V_{IN} = −1.0dBFS differential input, 1.0V internal reference, and DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			625	MHz
Conversion rate[1]					
DCS Enabled	Full	20		125	MSPS
DCS Disabled	Full	10		125	MSPS
CLK Period-Divide Mode (t_{CLK})		8			ns
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	2.5	4.3	5.7	ns
Divide-by-1 Mode, DCS Disabled	Full	3.7	4.2	4.3	ns
Divide-by-2 Mode Through Divide-by-8 Mode		0.85			ns
Aperture Delay (t_A)	Full	1.0			ns
Aperture Uncertainty (Jitter, t_J)	Full	0.07			ps rms
DATA OUTPUT PARAMETERS					
CMOS Mode					
Data Propagation Delay (t_{PD})	Full	2.9	3.7	4.4	ns
DCO Propagation Delay (t_{DCO})[2]	Full		3.3		ns
DCO to Data Skew (t_{SKEW})	Full	-0.63	-0.45	0	ns
LVDS Mode					
Data Propagation Delay (t_{PD})	Full	2.9			ns
DCO Propagation Delay (t_{DCO})[2]	Full		4.1		ns
DCO to Data Skew (t_{SKEW})	Full	-0.3	+0.4	+0.7	ns

CMOS Mode Pipeline Delay	Full	13	Cycle
LVDS Mode Pipeline Delay	Full	13/13.5	Cycle
Wake-Up Time[3]	Full	500	μs
Out-of-Range Recovery Time	Full	2	Cycle

1.Conversion rate is the clock rate after the divider.

2.Additional DCO delay can be added by writing to Bit 0 through Bit 4 in SPI Register 0x17.

3.Wake-up time is defined as the time required to return to normal operation from power-down mode.

Timing Specifications

Table 5.

Parameter	Conditions	Limit
SYNC TIMING REQUIREMENTS		
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.33 ns, typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.42 ns, typ
SPI TIMING REQUIREMENTS		
t_{DS}	Setup time between the data and the rising edge of SCLK	2.2 ns, min
t_{DH}	Hold time between the data and the rising edge of SCLK	2.2 ns, min
t_{CLK}	Period of the SCLK CSB	40.3 ns, min
t_S	Setup time between CSB and SCLK CSB	2.2 ns, min
t_H	Hold time between CSB and SCLK	2.2 ns, min
t_{HIGH}	SCLK pulse width high	10.2 ns, min
t_{LOW}	SCLK pulse width low	10.2 ns, min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10.2 ns, min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10.2 ns, min

Timing Diagrams

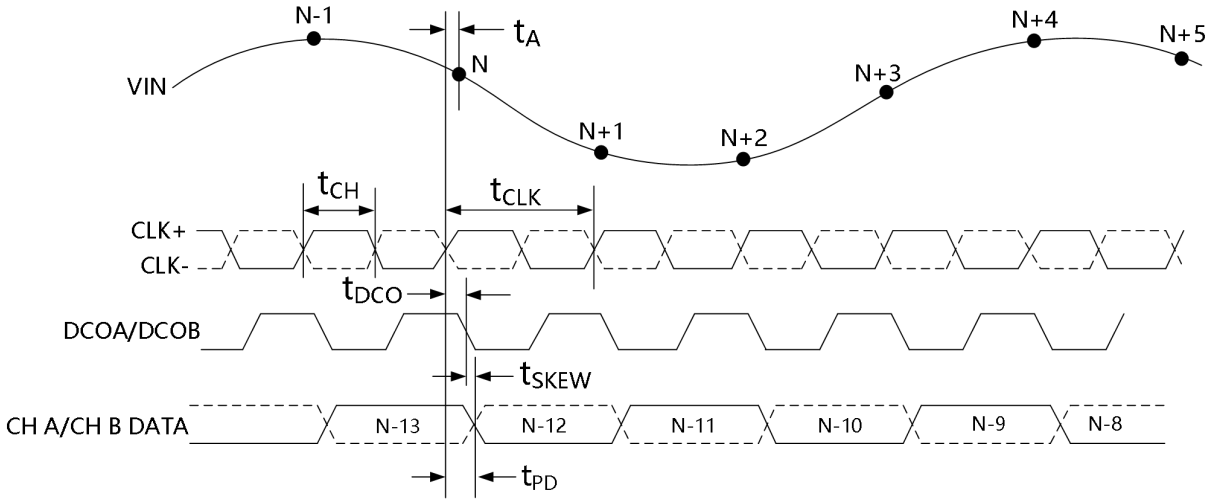


Figure 2. CMOS Default Output Mode Data Output Timing

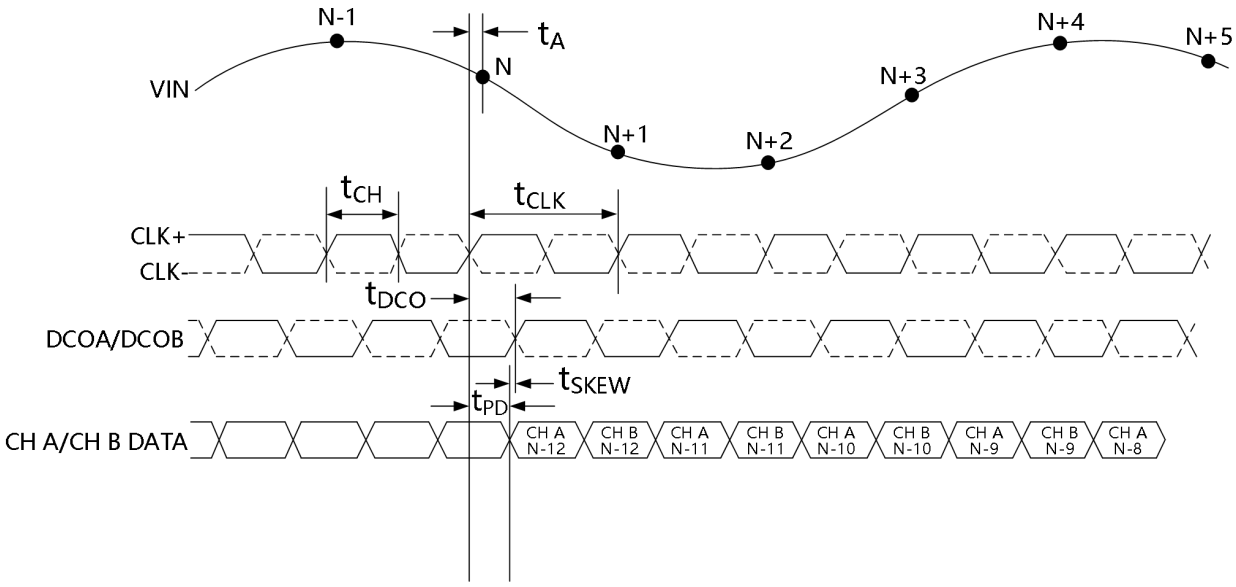


Figure 3. LVDS Mode Data Output Timing

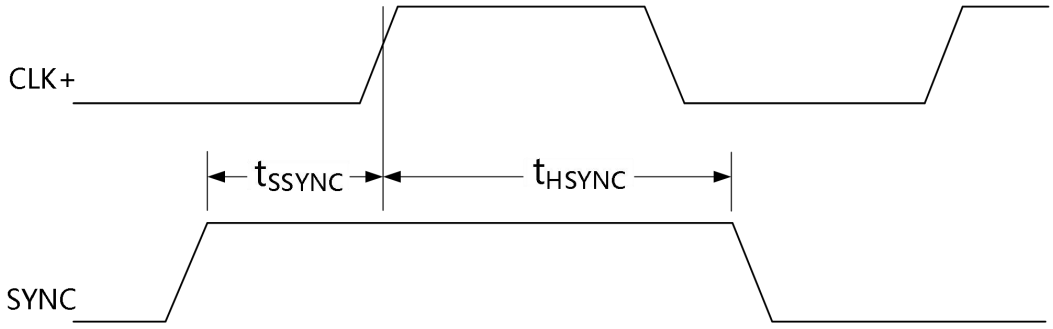
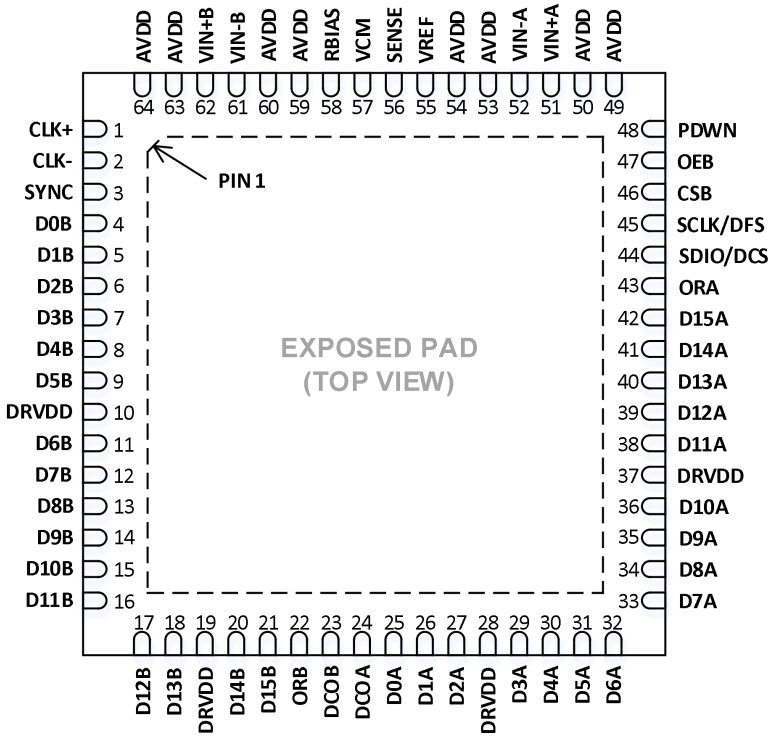


Figure 4. SYNC Input Timing Requirements

Absolute Maximum Ratings

Parameter	Range
AVDD，DRVDD to AGND	-0.3V to +2.0V
VIN±A/VIN±B，CLK±，SYNC，VREF，SENSE，VCM，RBIAS，CSB，OEB to AGND	-0.3V to AVDD+0.2V
SCLK/DFS，SDIO/DCS，PDWN，D0A/D0B-D15A/D15B，DCOA/DCOB to AGND	-0.3V to AVDD+0.2V
Maximum temperature for lead-free reflow soldering	260℃±5℃/20s
Junction temperature	150℃
Operating Temperature Range	-40℃ to 85℃
Storage Temperature Range	-65℃ to 150℃

Pin Configurations and Function Descriptions



NOTES.

THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

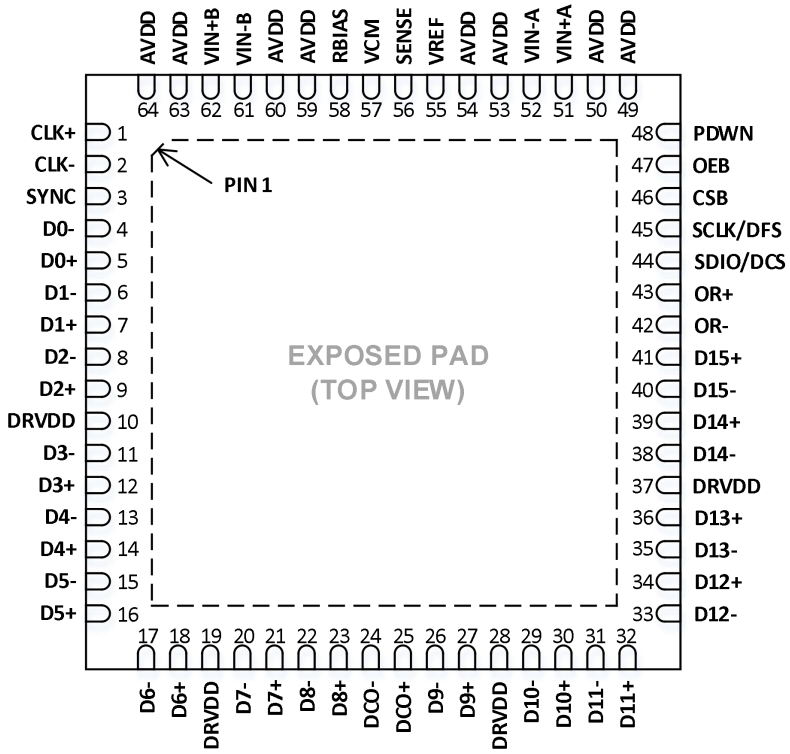
Figure 5. QFN Parallel CMOS Pin Configuration (Top View)

Table 6. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10,19,28,37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49,50,53,54,59,60,63,64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN-A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN-B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/output	Voltage Reference Input/Output.
56	SENSE	Input	Voltage Reference Mode Select.
58	RBIAS	Input/output	External Reference Bias Resistor.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input (+)
2	CLK-	Input	ADC Clock Input (−)
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
25	D0A (LSB)	Output	Channel A CMOS Output Data.
26	D1A	Output	Channel A CMOS Output Data.
27	D2A	Output	Channel A CMOS Output Data.
29	D3A	Output	Channel A CMOS Output Data.
30	D4A	Output	Channel A CMOS Output Data.
31	D5A	Output	Channel A CMOS Output Data.
32	D6A	Output	Channel A CMOS Output Data.
33	D7A	Output	Channel A CMOS Output Data.
34	D8A	Output	Channel A CMOS Output Data.
35	D9A	Output	Channel A CMOS Output Data.

36	D10A	Output	Channel A CMOS Output Data.
38	D11A	Output	Channel A CMOS Output Data.
39	D12A	Output	Channel A CMOS Output Data.
40	D13A	Output	Channel A CMOS Output Data.
41	D14A	Output	Channel A CMOS Output Data.
42	D15A (MSB)	Output	Channel A CMOS Output Data.
43	ORA	Output	Channel A Overrange Output.
4	D0B (LSB)	Output	Channel B CMOS Output Data.
5	D1B	Output	Channel B CMOS Output Data.
6	D2B	Output	Channel B CMOS Output Data.
7	D3B	Output	Channel B CMOS Output Data.
8	D4B	Output	Channel B CMOS Output Data.
9	D5B	Output	Channel B CMOS Output Data.
11	D6B	Output	Channel B CMOS Output Data.
12	D7B	Output	Channel B CMOS Output Data.
13	D8B	Output	Channel B CMOS Output Data.
14	D9B	Output	Channel B CMOS Output Data.
15	D10B	Output	Channel B CMOS Output Data.
16	D11B	Output	Channel B CMOS Output Data.
17	D12B	Output	Channel B CMOS Output Data.
18	D13B	Output	Channel B CMOS Output Data.
20	D14B	Output	Channel B CMOS Output Data.
21	D15B (MSB)	Output	Channel B CMOS Output Data.
22	ORB	Output	Channel B Overrange Output
24	DCOA	Output	Channel A Data Clock Output.
23	DCOB	Output	Channel B Data Clock Output.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			

47	OEB	Input	Output Enable Input (Active Low) in External Pin Mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.



NOTES.

The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.

Figure 6. QFN Interleaved Parallel LVDS Pin Configuration (Top View)

Table 7. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC power supply			
10,19,28,37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal)
49,50,53,54,59,60,63,64	AVDD	Supply	Analog Power Supply (1.8 V Nominal)
0	AGND, exposed thermal pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN-A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN-B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Voltage Reference Mode Select.
58	RBIAS	Input/Output	External Reference Bias Resistor.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input (+)
2	CLK-	Input	ADC Clock Input (−)
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
5	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0 (+)
4	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0 (-)
7	D1+	Output	Channel A/Channel B LVDS Output Data 1 (+)
6	D1−	Output	Channel A/Channel B LVDS Output Data 1 (-)
9	D2+	Output	Channel A/Channel B LVDS Output Data 2(+)
8	D2−	Output	Channel A/Channel B LVDS Output Data 2(-)
12	D3+	Output	Channel A/Channel B LVDS Output Data 3(+)
11	D3−	Output	Channel A/Channel B LVDS Output Data 3(-)
14	D4+	Output	Channel A/Channel B LVDS Output Data 4(+)
13	D4−	Output	Channel A/Channel B LVDS Output Data 4(-)

16	D5+	Output	Channel A/Channel B LVDS Output Data 5(+)
15	D5−	Output	Channel A/Channel B LVDS Output Data 5(-)
18	D6+	Output	Channel A/Channel B LVDS Output Data 6(+)
17	D6−	Output	Channel A/Channel B LVDS Output Data 6(-)
21	D7+	Output	Channel A/Channel B LVDS Output Data 7(+)
20	D7−	Output	Channel A/Channel B LVDS Output Data 7(-)
23	D8+	Output	Channel A/Channel B LVDS Output Data 8(+)
22	D8−	Output	Channel A/Channel B LVDS Output Data 8(-)
27	D9+	Output	Channel A/Channel B LVDS Output Data 9(+)
26	D9−	Output	Channel A/Channel B LVDS Output Data 9(-)
30	D10+	Output	Channel A/Channel B LVDS Output Data 10(+)
29	D10−	Output	Channel A/Channel B LVDS Output Data 10(-)
32	D11+	Output	Channel A/Channel B LVDS Output Data 11(+)
31	D11−	Output	Channel A/Channel B LVDS Output Data 11(-)
34	D12+	Output	Channel A/Channel B LVDS Output Data 12(+)
33	D12−	Output	Channel A/Channel B LVDS Output Data 12(-)
36	D13+	Output	Channel A/Channel B LVDS Output Data 13(+)
35	D13−	Output	Channel A/Channel B LVDS Output Data 13(-)
39	D14+	Output	Channel A/Channel B LVDS Output Data 14(+)
38	D14−	Output	Channel A/Channel B LVDS Output Data 14(-)
41	D15+ (MSB)	Output	Channel A/Channel B LVDS Output Data 15(+)
40	D15− (MSB)	Output	Channel A/Channel B LVDS Output Data 15(-)
43	OR+	Output	Channel A/Channel B LVDS Overrange Output 16(+)
42	OR−	Output	Channel A/Channel B LVDS Overrange Output 16(-)
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output(+)
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output(-)
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.

46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low) in External Pin Mode.
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

Typical Performance Characteristics

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate 125MSPS, 2V p-p differential input, V_{IN} = −1dBFs, T_A = 25°C, unless otherwise noted.

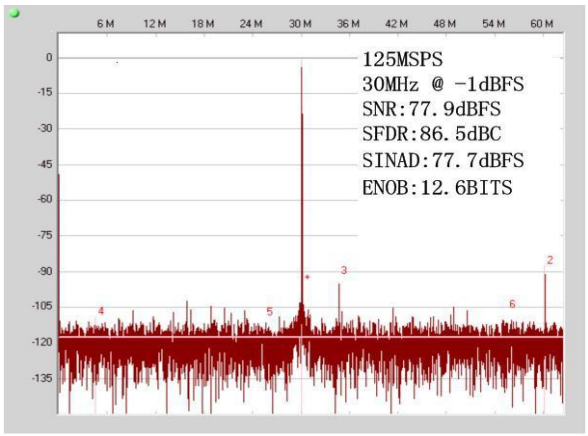


Figure 7. Single-Tone FFT with f_{IN} = 30MHz

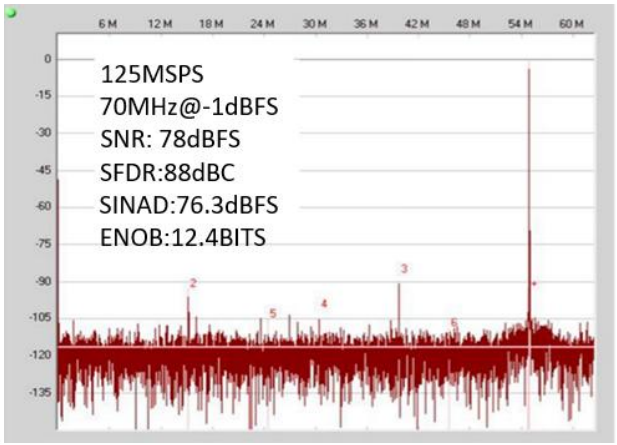


Figure 8. Single-Tone FFT with f_{IN} = 70MHz

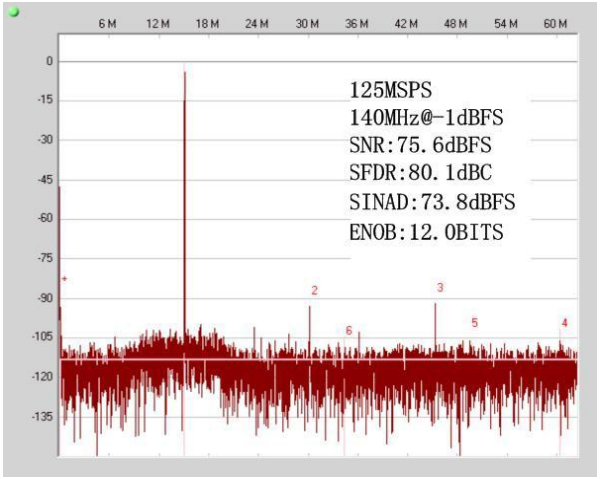


Figure 9. Single-Tone FFT with f_{IN} = 140MHz

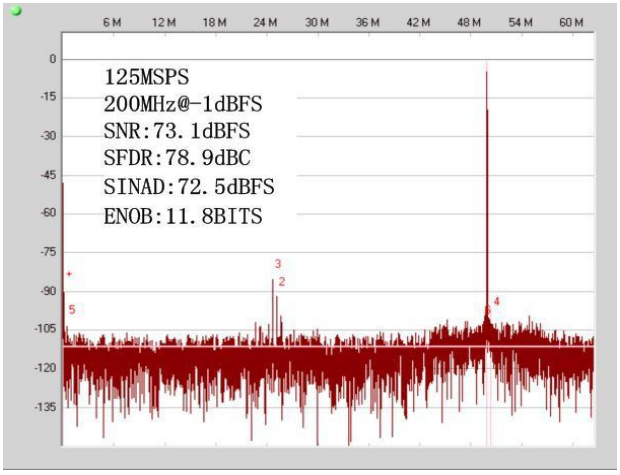


Figure 10. Single-Tone FFT with f_{IN} = 200MHz

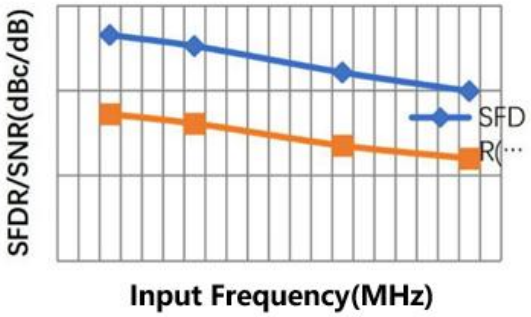


Figure 11 SNR/SFDR vs. Input Frequency
(fin=70MHz，Dither Off)

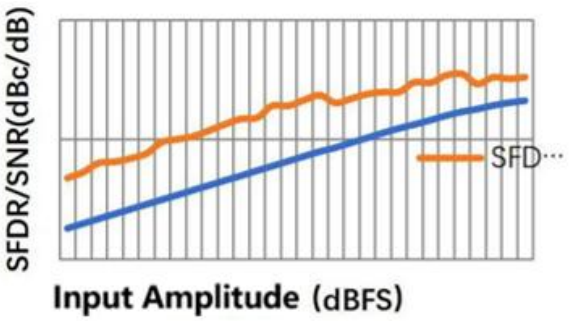


Figure 12 SNR/SFDR vs. Input Amplitude
(fin=70MHz，Dither Off)

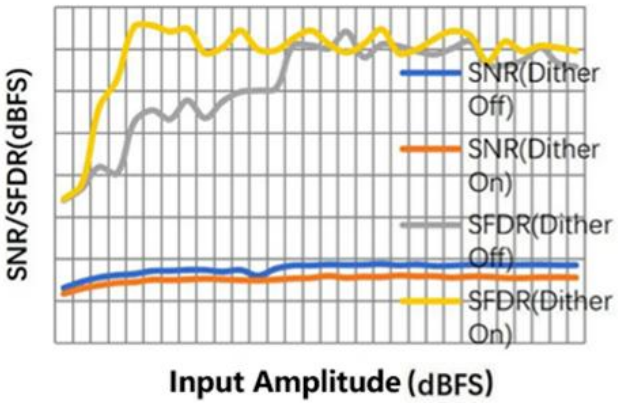


Figure 13 SNR/SFDR vs. Input Amplitude(fin=30.1MHz)

Applications Information

- **Input Common Mode**

The ADC analog inputs are not internally dc biased. In accoupled applications, the user must provide this bias externally. An on-chip, common-mode voltage reference is available from either the VCM pin or autonomous setting if V_{CM} = 0.5×AVDD (or 0.9 V) are met. When the common-mode voltage of the analog input is set by the V_{CM} pin voltage (typically 0.5 × AVDD). The V_{CM} pin must be decoupled to ground by a 0.1μF capacitor （Figure 13, Figure 14）

- **Differential Input Configurations**

There are two configurations:

1. The input configuration uses differential transformer coupling. An example is shown in Figure 13. To bias the analog input, the V_{CM} voltage can be connected to the center tap of the secondary winding of the transformer.

2. The input configuration uses differential double balun coupling (see Figure 14). In this configuration, the input is ac-coupled, and the CML is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver. Table 8 displays recommended values to set the RC network.

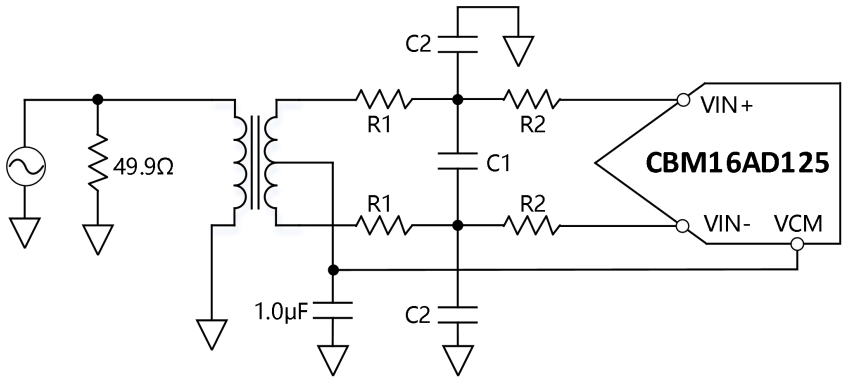


Figure 14. Differential Transformer-Coupled input Configuration

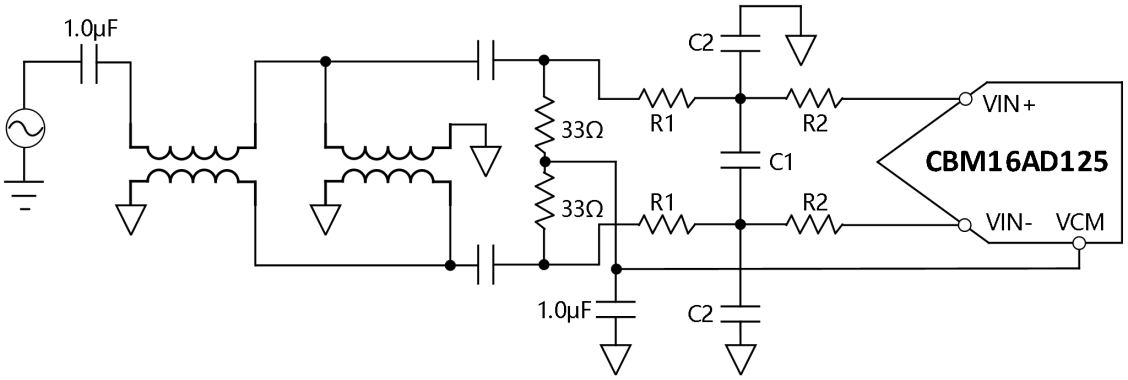


Figure 15. Differential double-Balun-Coupled input Configuration

Table 8. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Shunt (pF)	R2 Series (Ω)	C2 Shunt (pF)
0 to 100	10~33	5	15	15
100 to 300	10	5	10	10

- **Reference voltage connection**

The reference of CBM16AD125 have multiple configuration modes (see table 10).

The first: the SENSE pin is tied to ground, the reference amplifier switch connects to the internal voltage divider, see Figure 15, thus the V_{REF} is set to 1.0V (full-scale input for 2V p-p). In this mode shown in table 9 the SENSE is tied to ground or adjust full scale through SPI port.

The second: the chip connects to an external resistance voltage divider, the voltage shown in Figure 16 is V_{REF}=0.5*(1+R_2/R_1). V_{REF} can be changed by adjusting the ratio of R_2 and R_1, and the ratio range of R_2 / R_1 is 0.5 ~ 1.

No matter which of the above modes is used, the voltage input range of the ADC is always twice the voltage of the reference voltage pin (V_{REF}).

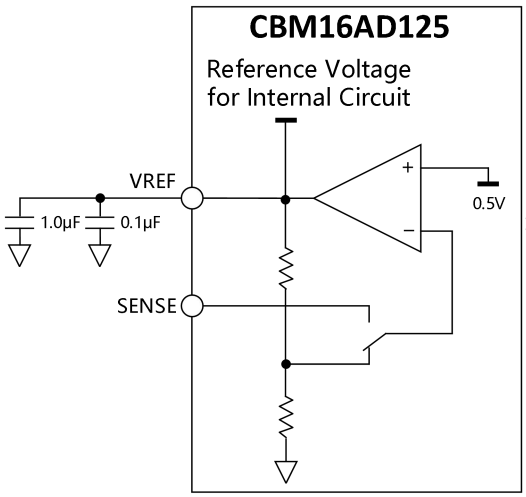


Figure 15. SENSE pin connects to ground mode (V_{REF} internal configuration mode)

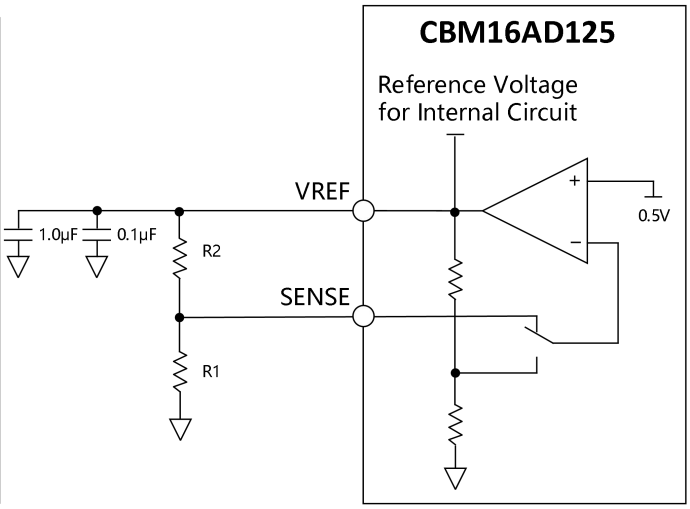


Figure 16. External resistance string mode (V_{REF} external configuration mode)

Table 9. V_{REF} Register configuration

Register address	Register name	Bit7	Bit6	Bit5~Bit0	Default value(Hexadecimal)
0x18	V_{REF} selection	00 Disable,01=1.5V p-p 10=1.75Vp-p,11=2V p-p (default)		Disable	0XC0

Table 10. Summary of Reference voltage configuration

Selected mode	SENSE Voltage	Corresponding VREF (V)	Corresponding difference (Vp-p) range
External reference voltage	AVDD	N/A	2* External reference voltage
Programmable reference voltage	0.2 to V_{REF}	0.5*(1+R2/R1)	2*V_{REF}
Internal fixed reference voltage	AGND to 0.2V	1.0	2.0

- **Clock Input**

The CBM16AD125 can use CMOS, LVDS, LVPECL or sine wave signal as clock input signal. Pin CLK+ and Pin CLK− have internal bias and external offset is not required. Figure 17 and figure 18 show two principal solution providing clock signals (Clock rate could up to 625 MHz) for

CBM16AD125. Using RF balun or RF transformer, Single ended signal of Low-Jitter clock source can convert to differential signal. The RF balun configuration is recommended for clock frequencies 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200MHz. The back-to-back Schottky diodes across the transformer/balun' s secondary windings limit the clock excursions into the CBM16AD125 to approximately 0.8 V p-p differential.

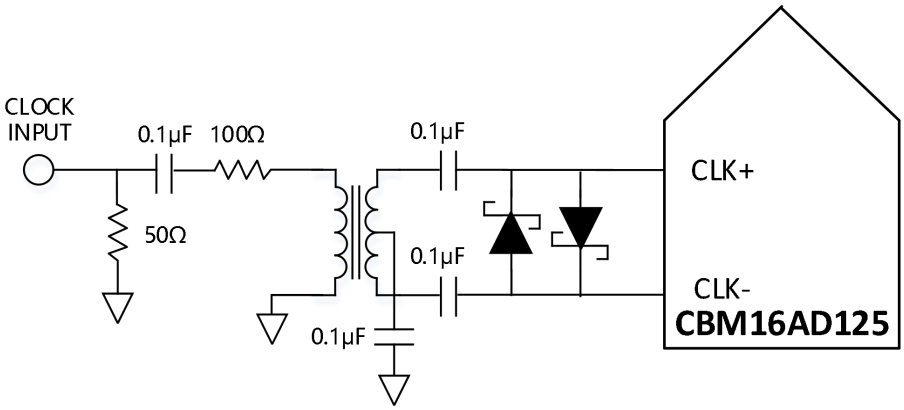


Figure 17. Clock input for transformer configuration

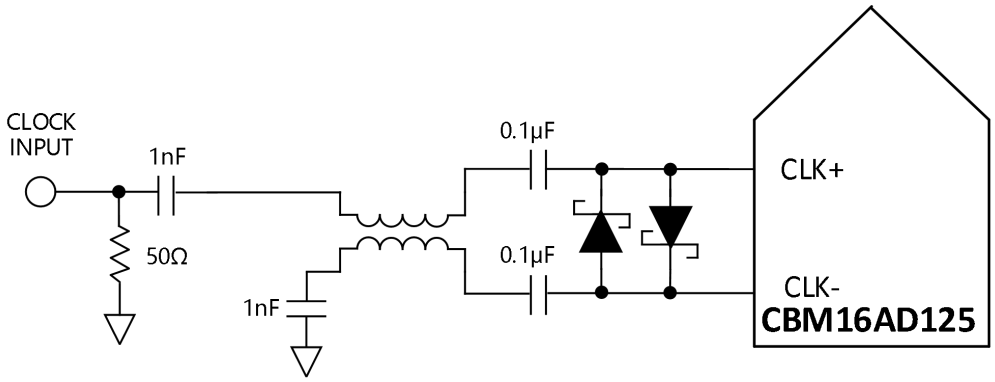


Figure 18. Baron configured clock

- **Memory Map Registers**

Address	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x00	SPI port configuration (global)	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	R/W
0x01	Chip ID (global)	8-bit Chip ID [7:0]								0x32	R
0x02	Speed grade(global)	Open	Open	Speed grade ID 01-125MSPS 10-105MSPS 11-80MSPS		Open	Open	Open	Open	0x10	R

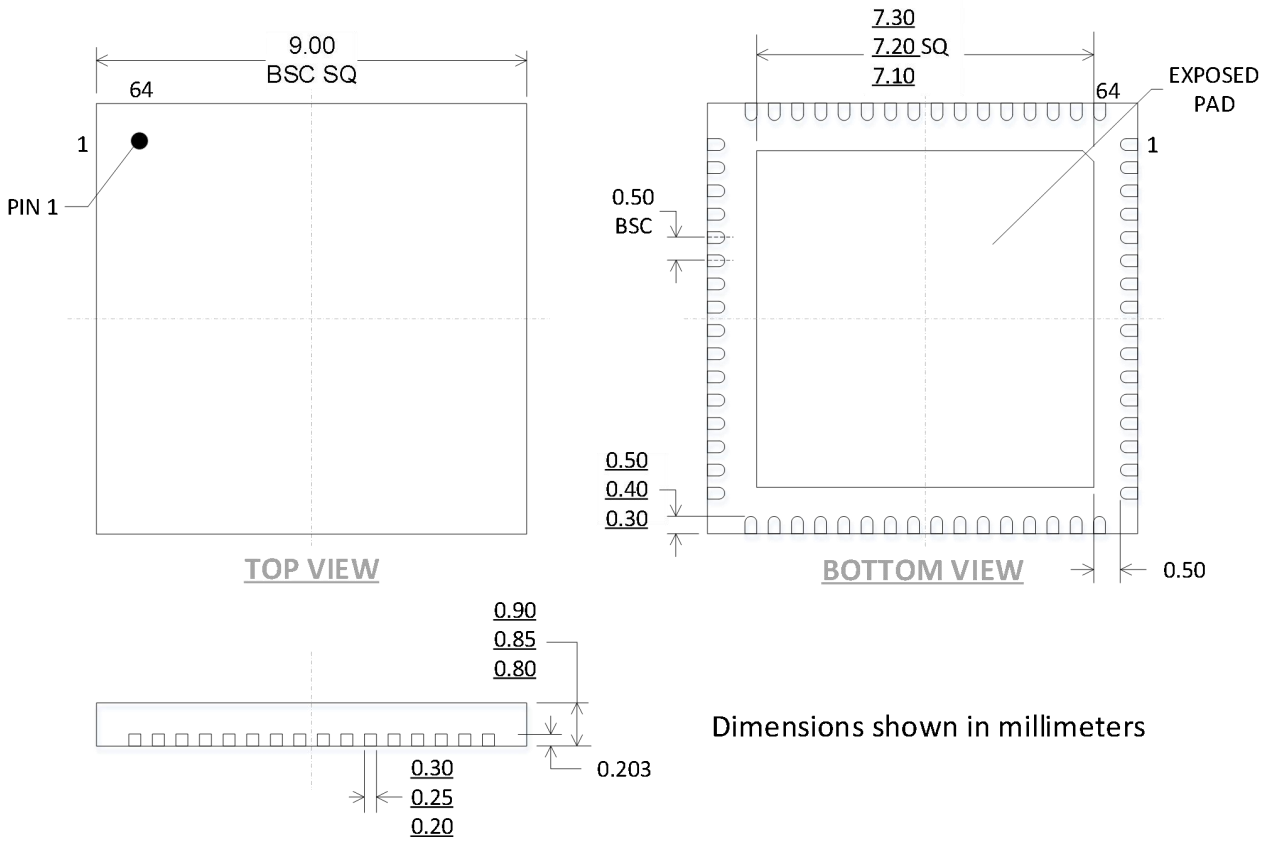
0x05	Channel index	Open	Open	Open	Open	Open	Open	Data Channel B(Default)	Data Channel A(Default)	0x03	R/W
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	1-Transfer	0x00	W
0x08	Power modes (local)	1	Open	External power-down pin function 0 = pdwn 1 = stndby	Open	Open	Open	Internal power-down mode (local) 00 = normal operation 01 = full power-down 10 = standby 11 = normal operation		0x80	R/W
0x09	Global clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer: 1=Open 0=Close	0x01	R/W
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio 000 = No frequency division 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	R/W
0x0D	Test mode (local)	Open	Open	Reset PN long gen	Reset PN short gen	Open	Output test mode 000 = off (default) 001 = midscale short 010 = positive FS 011 = negative FS 100 = alternating checkerboard 101 = PN long sequence 110 = PN short sequence 111 = one/zero-word toggle			0x00	R/W
0x0E	BIST enable (global)	Open	Open	Open	Open	Open	Reset BIST sequence	Open	BIST enable 1=Open 0=Close	0x04	R/W

0x0F	ADC input (global)	Open	Open	Open	Open	Open	Open	Open	Common-mode servo enable	0x00	R/W
0x10	Offset adjust(local)	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	R/W
0x14	Output mode	Drive strength 0 = ANSI LVDS; 1 = reduced swing LVDS (global)	Output type 0 = CMOS 1 = LVDS (global)	CMOS output interleave enable (global)	Output enables (local)	Open	Output invert (local) 1=Open 0=Close	Output format 00 =offset binary 01 = twos complement 10 = gray code 11=offset binary		0x00	R/W
0x16	Clock phase control (global)	Invert DCO clock 1=Open 0=Close	Open	Open	Open	Open	Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			0x00	R/W
0x17	DCO output delay (global)	Open	Open	Open	DCO clock delay (delay = 2500 ps × register value/31) 00000 = 0 ps 00001 = 81 ps 00010 = 161 ps ... 11110 = 2419 ps 11111 = 2500 ps					0x00	R/W
0x18	VREF select (global)	Reference voltage selection 00 = 1.25 V p-p 01 = 1.5 V p-p 10 = 1.75 V p-p 11 = 2.0 V p-p		Open	Open	Open	Open	Open	Open	0xC0	R/W
0x24	BIST signature LSB (local)	BIST signature [7:0]								0x00	R
0x25	BIST signature MSB (local)	BIST signature [15:8]								0x00	R

0x30	Dither enable (local)	Open	Open	Open	Dither enable: 1=Open 0=Close	Open	Open	Open	Open	0x00	R/W
0x100	Sync control (global)	Open	Open	Open	Open	Open	Single / multiple synchronization selection: 1= Single synchronization 0= Continuous synchronization	Clock divider sync enable: 1=Open 0=Close	Master sync enable: 1= Synchronous on 0= Synchronous off	0x00	R/W
0xF5[1]	Trimming										

[1]The trimming register 0xF5 should be configured as: 0xF5=0x00

Outline Dimensions



Dimensions shown in millimeters

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION	MAKING INFORMATION
CBM16AD80Q		-40℃~85℃	QFN-64	Tray，260	
CBM16AD105Q		-40℃~85℃	QFN-64	Tray，260	
CBM16AD125Q		-40℃~85℃	QFN-64	Tray，260	