Features

- Resolution: 16 bits
- Power supply voltage: 3.3V/1.8V
- Sampling rate: 250MSPS(Max)
- SNR: 72dBFS(170 MHz @ 250 MSPS)
- SFDR: 89dBc(170 MHz @ 250 MSPS)
- 60 fs rms jitter
- DNL=±0.5LSB（Typ）
- INL=±3.5LSB（Typ）
- Differential analog input range≤2.5VPP
- SPI Function
- DDR LVDS output（ANSI-644 compatible）
- Built-in clock with stable duty cycle and clock output
- Packaging type: QFN72
- AD9467-250 P2P Compatible

Application

- Communication
- Receiver
- Base station
- Spectral analysis
- Broadband wireless
- Radar
- Infrared imaging
- Power amplifier linearization
- Image processing

Description

The CBM94AD67 is a 16-bit, monolithic, IF sampling analog-to-digital converter (ADC). It is optimized for high performance over wide bandwidths and ease of use. The product operates at a 250 MSPS conversion rate and is designed for wireless receivers, instrumentation, and test equipment that require a high dynamic range.

The ADC requires 1.8 V and 3.3 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are LVDS compatible (ANSI-644 compatible) and include the means to reduce the overall current needed for short trace distances.

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The CBM94AD67 is available in a Pb-free, 72-lead, QFN specified over the −40°C to +85°C industrial temperature range.

Datalog

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2024.12.19	Update some measured parameters in the product specifications table."	Error update	WW	LYL	

Functional Block Diagram

The main function of this product is to convert input analog signals into 16 bit parallel digital signal outputs, mainly used for collecting high-frequency broadband signals. The power supply voltage is 3.3V/1.8V, and the converter includes front-end buffer, pipeline circuit, logic calibration, output IO, clock processing circuit, output control, reference and other functional unit circuits. The functional block diagram of this product is shown in Figure 1, and the timing is shown in Figure 2.

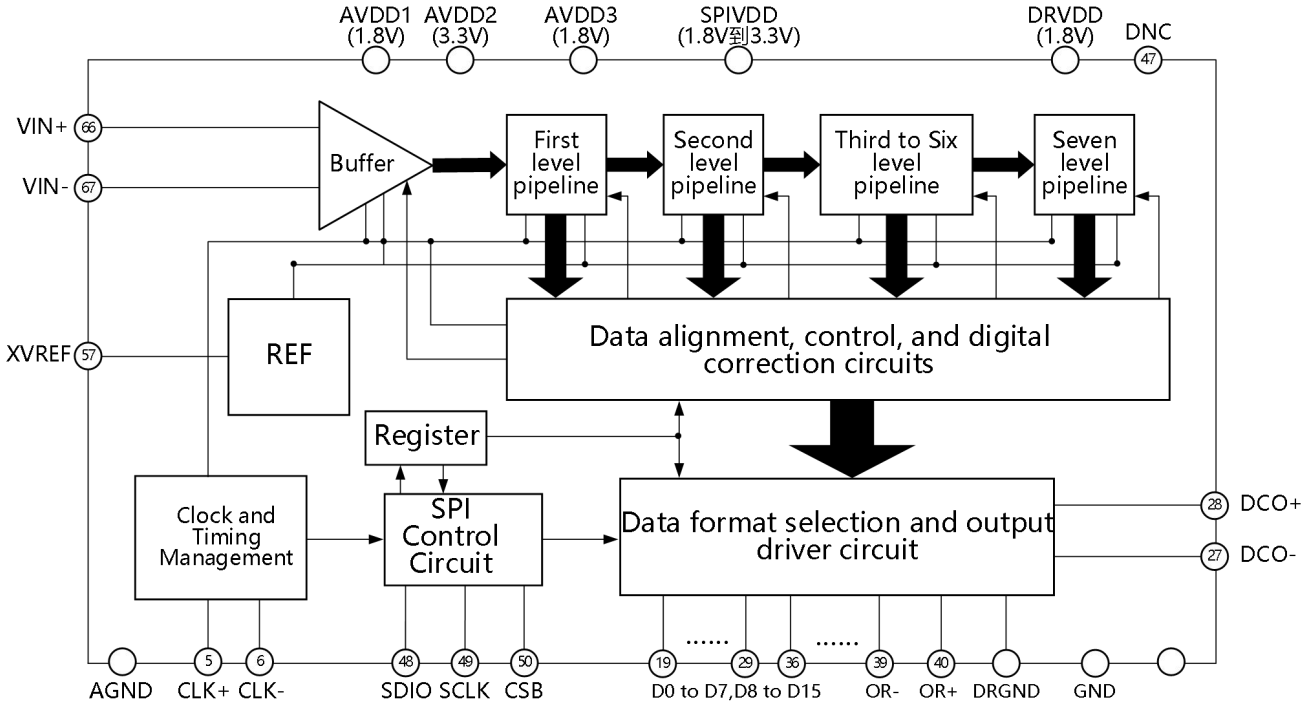


Figure 1.Functional Block Diagram

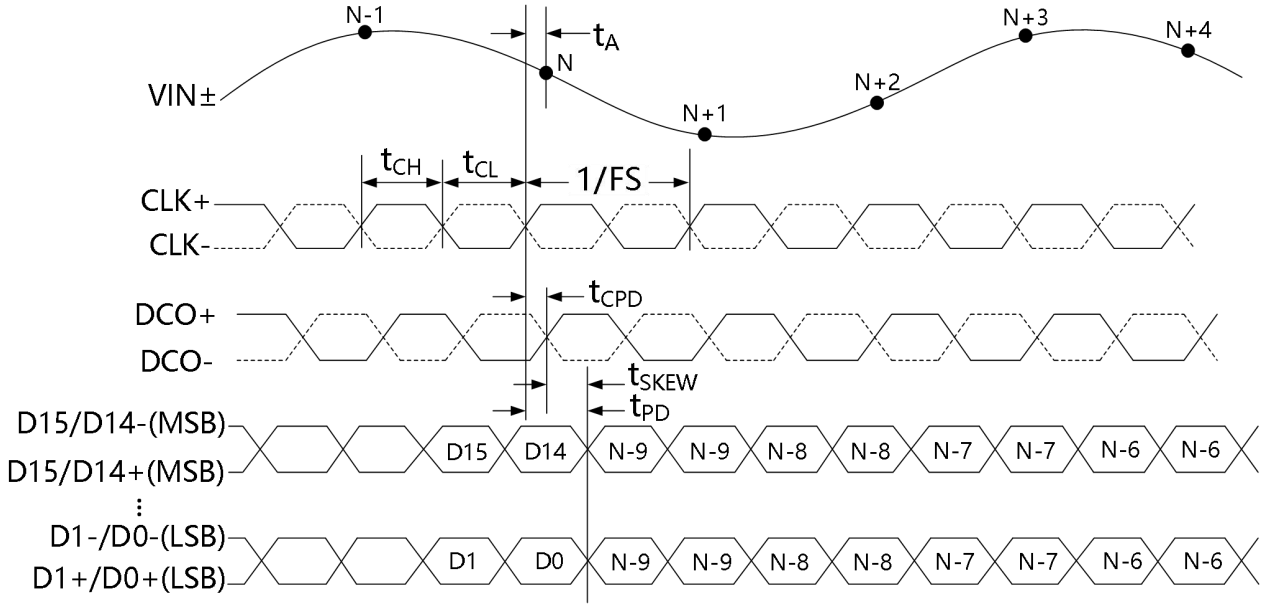
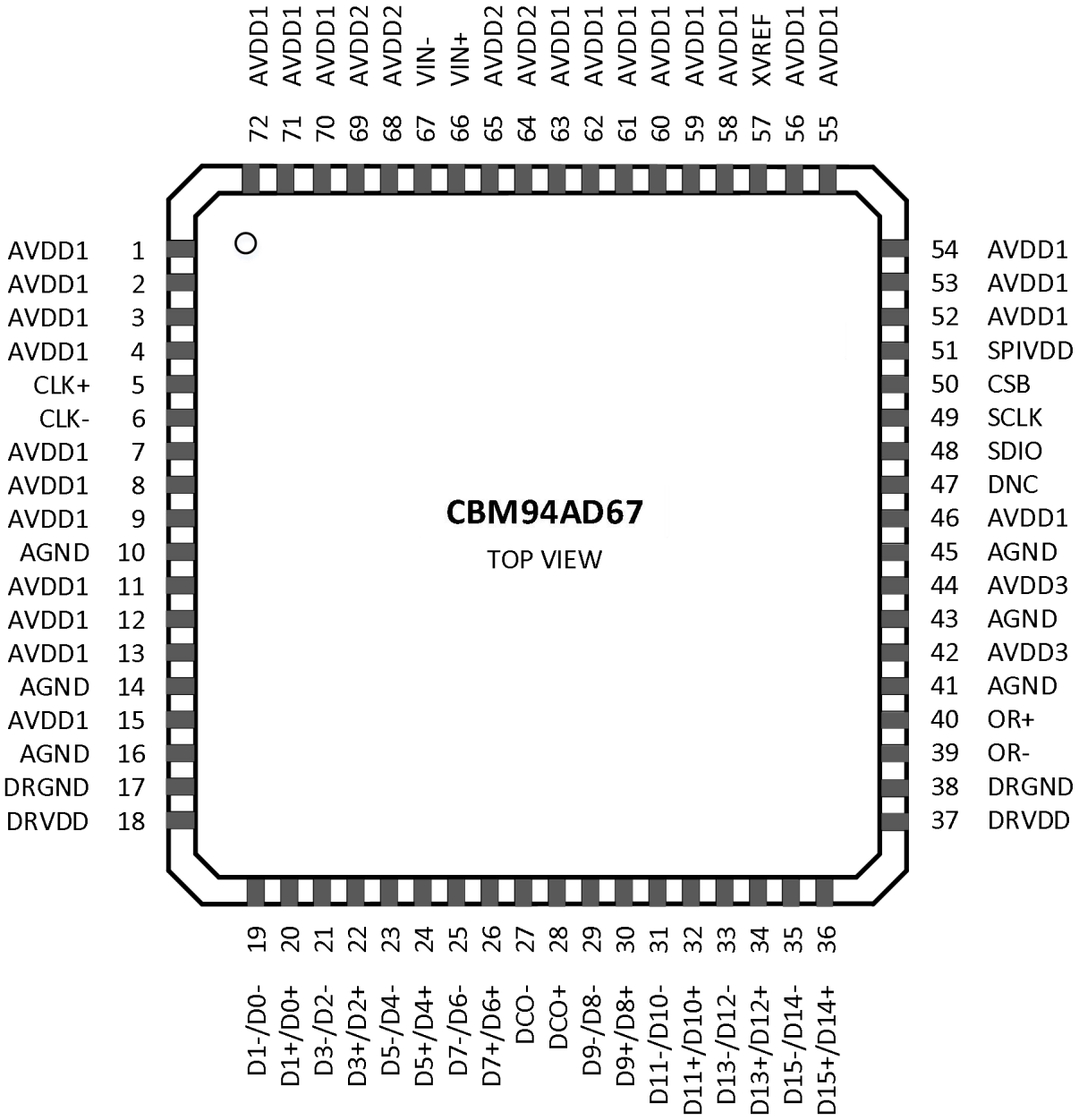


Figure 2.16-Bit Output Data Timing

Pin Configuration and Function Descriptions

Pin Configuration



CBM94AD67 Pin Configuration

Figure 3.Pin Configuration,Top View

Pin Definition

Table 1.Pin Function Descriptions

Pin Num	Symbol	Function
10,14,16,41,43,45	AGND	Analog Ground.
1, 2, 3, 4, 7, 8, 9, 11, 12, 13, 15, 46, 52, 53, 54, 55, 56, 58, 59, 60, 61, 62, 63, 70, 71, 72	AVDD1	1.8V Analog Supply.
64,65,68,69	AVDD2	3.3V Analog Supply.
42,44	AVDD3	1.8V Analog Supply.
51	SPIVDD	1.8 V or 3.3 V SPI supply.
17,38	DRGND	Digital Output Driver Ground.
18,37	DRVDD	1.8 V Digital Output Driver Supply.
67	VIN-	Analog Input Complement.
66	VIN+	Analog Input True.
6	CLK-	Clock Input Complement.
5	CLK+	Clock Input True.
19	D1-/D0-	D1 and D0 (LSB) Digital Output Complement.
20	D1+/D0+	D1 and D0 (LSB) Digital Output True.
21	D3-/D2-	D3 and D2 Digital Output Complement.
22	D3+/D2+	D3 and D2 Digital Output True.
23	D5-/D4-	D5 and D4 Digital Output Complement.
24	D5+/D4+	D5 and D4 Digital Output True.
25	D7-/D6-	D7 and D6 Digital Output Complement.
26	D7+/D6+	D7 and D6 Digital Output True.
29	D9-/D8-	D9 and D8 Digital Output Complement.
30	D9+/D8+	D9 and D8 Digital Output True.
31	D11-/D10-	D11 and D10 Digital Output Complement.
32	D11+/D10+	D11 and D10 Digital Output True.
33	D13-/D12-	D13 and D12 Digital Output Complement.
34	D13+/D12+	D13 and D12 Digital Output True.
35	D15-/D14-	D15 and D14 Digital Output Complement.
36	D15+/D14+	D15 and D14 Digital Output True.

27	DCO-	Data Clock Digital Output Complement.
28	DCO+	Data Clock Digital Output True.
39	OR-	Out-of-Range Digital Output Complement.
40	OR+	Out-of-Range Digital Output True.
47	DNC	Do Not Connect (Leave Pin Floating).
48	SDIO	Serial Data Input/Output.
49	SCLK	Serial Clock.
50	CSB	Chip Select Bar.
57	XVREF	External VREF Option.

Absolute Maximum Ratings

Parameter	Rating
AVDD to AGND	-0.3V to +2.0V
DRVDD to DRGND	-0.3V to +2.0V
AGND to DRGND	-0.3V to +0.3V
AVDD to DRVDD	-2.0V to +2.0V
D0+/D0− Through D11+/D11− to DRGND	−0.3 V to DRVDD + 0.2 V
DCO+, DCO− to DRGND	−0.3 V to DRVDD + 0.2 V
OR+, OR− to DRGND	−0.3 V to DRVDD + 0.2 V
CLK+ to AGND	−0.3 V to AVDD + 0.2 V
CLK - to AGND	−0.3 V to AVDD + 0.4 V
VIN+ to AGND	−0.3 V to AVDD + 0.4 V
VIN- to AGND	−0.3 V to AVDD + 0.2 V
CML to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SDIO to DRGND	−0.3 V to DRVDD + 0.2 V
PDWN to AGND	−0.3 V to DRVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.2 V
Operating Temperature Range	-40℃ to +85℃
Lead Temperature (Soldering, 10 sec)	300℃
Junction Temperature	150℃
Storage Temperature Range	-65℃ to +125℃

Specifications

Analog input peak-to-peak maximum 2.5V, AVDD1 = 1.8V, AVDD3 = 1.8V, DRVDD = 1.8V, AVDD2 = 3.3V, G_{NDA} = G_{NDD} = 0, -40 ° C ≤ T_A ≤ + 85 ° C, unless otherwise specified,

Table 2.

Parameter[1]	Symbol	Test conditions and instructions	CBM94AD67-200			CBM94AD67-250			Unit
			Min	Typ	Max	Min	Typ	Max	
Resolution	--	--		16			16		Bits
Integral Nonlinearity (INL)	E_L	f_{IN}=10MHz	-16	±3.5	16	-16	±3.5	16	LSB
Differential Nonlinearity (DNL)	E_{DL}	f_{IN}=10MHz	-1	±0.5	1.5	-1	±0.5	1.5	LSB
Offset Error	E_O	--	-250	-5	250	-250	-5	250	LSB
Gain Error	E_G	--	-8	-1.8	8	-8	-1.8	8	%FSR
Full Power Bandwidth	FPBW	--	--	900	--	--	900	--	MHz
Aperture Uncertainty (Jitter)	AUJ		--	60	--		60		fs rms
Power Dissipation	P_W	--	--	--	1.8	--	1.295	1.8	W
Signal-to-Noise RATIO (SNR)	SNR	f_{IN}=70MHz@A_{IN}=−1 dB	70	74.24	--	70	74.42	--	dBFS
		f_{IN} =140MHz@A_{IN}=−1 dB	69	72.35	--	69	72.75	--	
		f_{IN}=170MHz@A_{IN}=−1 dB	69	71.82	--	69	72.03	--	
Signal-to-Noise and Distortion Ratio (SINAD)	SINAD	f_{IN}=70MHz@A_{IN}=−1 dB	70	74.20	--	70	74.24	--	dBFS
		f_{IN}	69	72.52	--	69	72.55	--	

		=140MHz@A_{IN}=−1 dB							
		f_{IN}=170MHz@A_{IN}=−1 dB	69	71.84	--	69	71.87	--	
Effective Number of Bits (ENOB)	ENOB	f_{IN}=70MHz@ A_{IN}=−1 dB	11.2	12.00	--	11.2	12.04	--	Bits
		f_{IN} =140MHz@ A_{IN}=−1 dB	11	11.75	--	11	11.76	--	
		f_{IN}=170MHz@ A_{IN}=−1 dB	11	11.63	--	11	11.65	--	
Spurious-Free Dynamic Range (SFDR) (Including Second and Third Harmonic Distortion)[2]	SFDR	f_{IN}=70MHz@ A_{IN}=−1 dB	77	90.5	--	77	91.31	--	dBFS
		f_{IN} =140MHz@ A_{IN}=−1 dB	75	88	--	75	89.04	--	
		f_{IN} =170MHz@ A_{IN}=−1 dB	75	89	--	75	89.05	--	
Sampling Rate	SR	--	50	--	200	50	--	250	MSPS

Typical Performance Characteristics

The INL and DNL test curves are shown in Figure 4. The FFT with an input analog frequency of 100MHz and a sampling rate of 250MSPS is shown in Figure 5. The FFT with an input analog frequency of 170MHz and a sampling rate of 250MSPS is shown in Figure 6. The FFT with an input analog frequency of 230MHz and a sampling rate of 250MSPS is shown in Figure 7. The FFT with an input analog frequency of 300MHz and a sampling rate of 250MSPS is shown in Figure 8. The bandwidth test is shown in Figure 9.

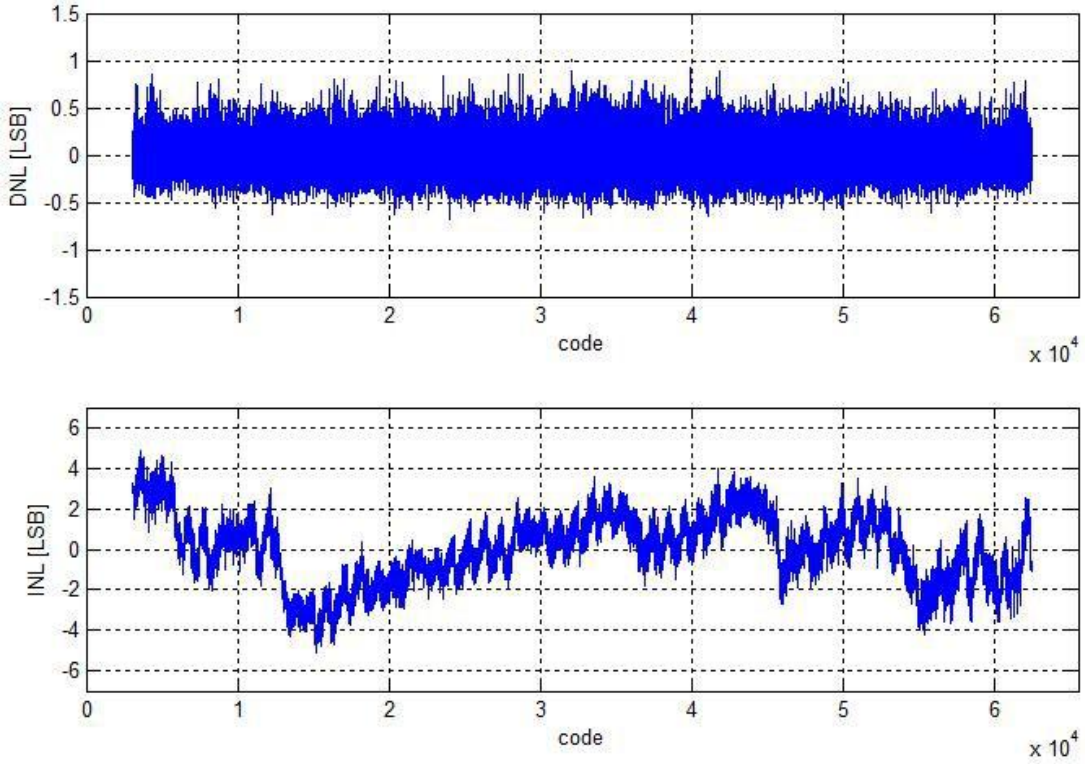


Figure 4.Typical test diagrams for INL and DNL

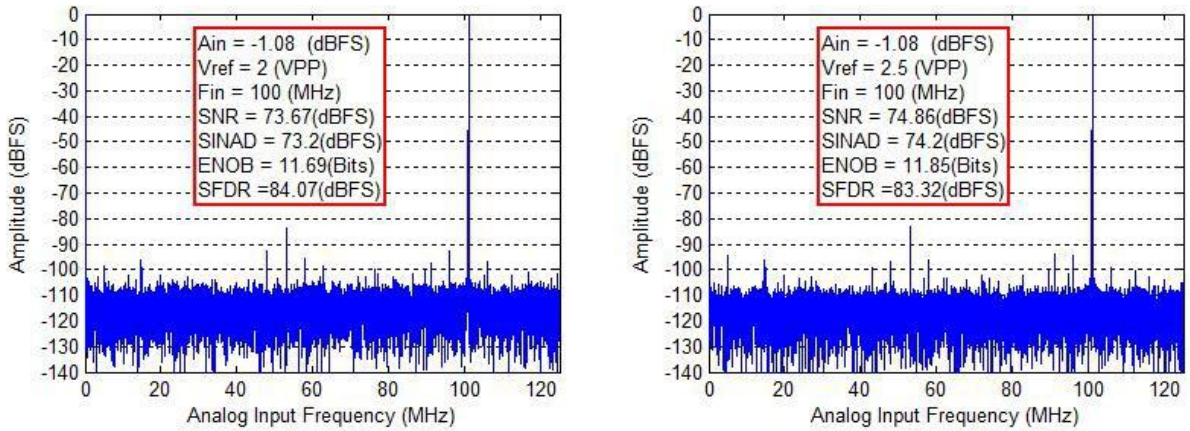


Figure 5.FFT characteristics: Analog input frequency 100MHz, sampling rate 250MSPS

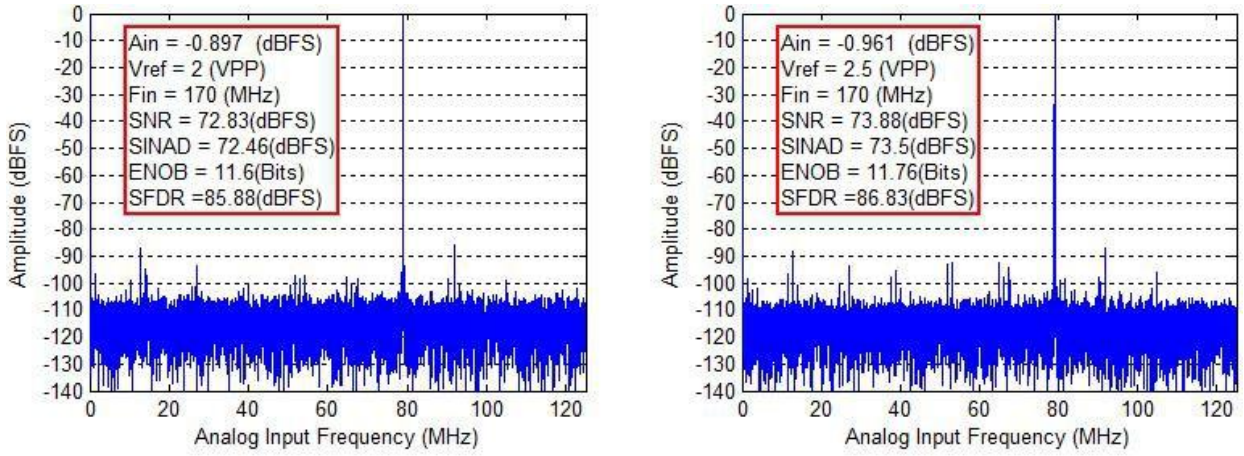


Figure 6. FFT characteristics: Analog input frequency 170MHz, sampling rate 250MSP

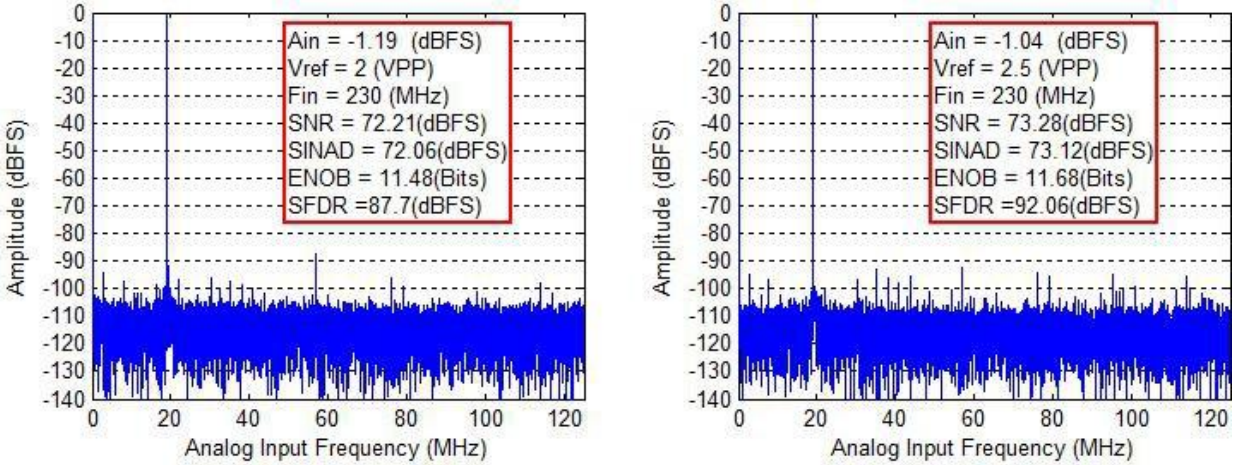


Figure 7. FFT characteristics: Analog input frequency 230MHz, sampling rate 250MSPS

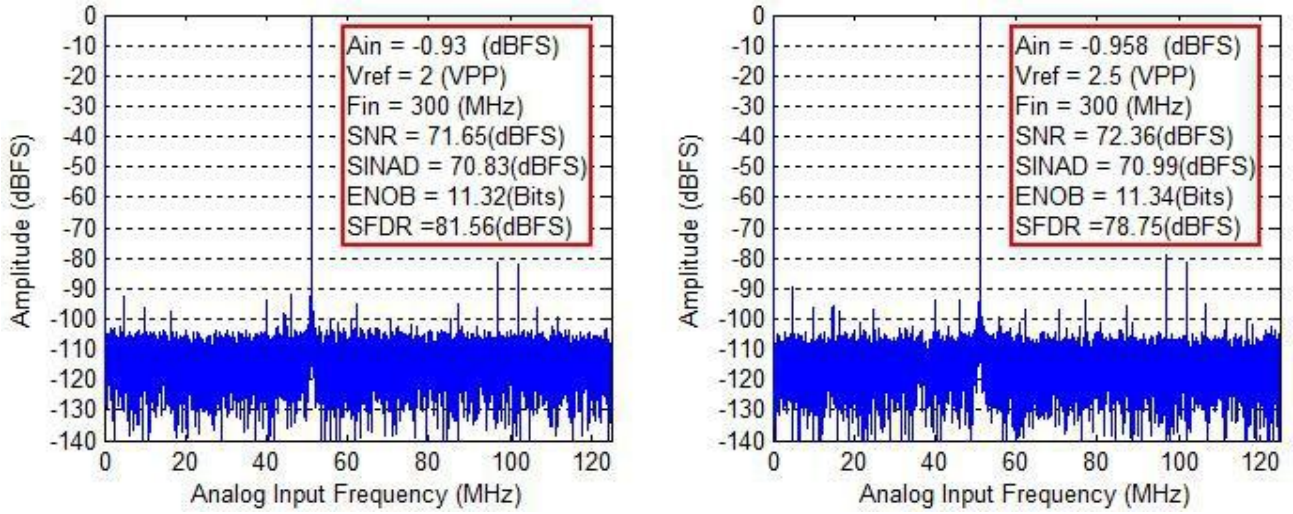


Figure 8. FFT characteristics: Analog input frequency 300MHz, sampling rate 250MSPS

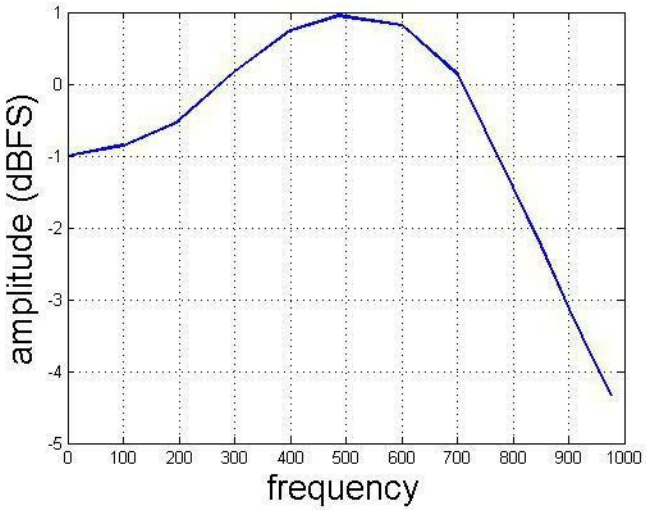


Figure 9. Full power bandwidth characteristics

Control Function

The control function of this product is mainly achieved through SPI, and the SPI register definition is shown in the table below.

Table 3.Register Map

Addr (Hex)	Parameter Name	Bit7(MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)	Default Value (Hex)	Default Notes/ Comments
08	modes	X	X	X	X	X	X	Internal power-down mode 00 = chip run (default) 01 = full power-down		0X00	Determines various generic modes of chip operation.
09	clock	X	X	X	X	X	X	X	1=DCS	0X01	
0C	enhanced Mode	X	X	X	X	X	X	X	1=random mode	0X01	Enable Random Mode
0D	test_io	X	X	Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	X	Output test mode 0000=off(default) 0001=midscale short 0010=+FS short 0011=-FS short 0100=checker-boardoutput 0101=PN23 sequence 0110=PN9 sequence 0111=1/0 word toggle			0X00	When this register is set, the test data is placed on the output pins in place of normal data.
0E	BIST	X	X	X	X	X	BIST boot up	X	BIST enable	0X00	BIST mode configuration
0F	ADC Input	XVREF 0=off(default) 1=on					Analog disconnect 0=off default 1=on			0X00	Analog input functions.
10	offset									0X00	Offset adjustment; combine 01A0 and 01A1 registers.

14	output_mode	X	0	X	Digital output disable 1 = on 0 = off (default)	1= DDR enable	Output invert 1 = on 0 = off (default)	Data format select 00 = offset binary (default) 01 = twos complement 10 = Gray code		0X08	Configures the outputs and the format of the data.
15	output_adjust	X	X	X	X	Coarse LVDS adjust (0=3.0 mA;1=1. 71mA(d efault)	Output current drive adjust: 001=3.0mA(default) 010=2.79mA 011=2.57mA 100=2.35mA 101=2.14mA 110=1.93mA 111=1.71mA			0X00	Determines LVDS or other output properties.
16	output_phase	DCO output invert 1=on 0=off	X	X	X	X	X	X	X	0X00	Determines digital clock output phase.
17	Output delay	enable 1=on 0=off	X	X	delay adjustment					0X00	Adjusting the delay of the output clock
18	Vref	X	X	X	X	Input full-scale range adjust 0000=2.0V_{p-p} 0110=2.1V_{p-p} 0111=2.2V_{p-p} 1000=2.3V_{p-p}				0X0A	Adjust Vref

						1001=2.4V_{p-p}					
						1010=2.5V_{p-p}(default)					
2C	analog_input	X	X	X	X	X	Input coupling mode 0 = ac coupling (default) 1 = dc coupling	X	X	0X00	Determines the input coupling mode.
36	Buffer Current Select 1	001000=+80%						1	0	0X22	
107	Buffer Current Select 2	001000=+80%(default)						X	X	0X20	

Application Descriptions

- **Input Signal**

The analog input front-end of the A/D converter is a differential buffer, and to achieve the best dynamic performance, the source impedance of the differential analog terminal should be matched. It is best to connect a small resistor in series at the input end to reduce the transient current peak of the driving source output stage. At the same time, low Q value inductors or magnetic beads are placed on each input to reduce the differential capacitance of the analog input, thereby maximizing the bandwidth of the A/D converter. At high IF frequencies, it is necessary to use low Q value inductors or magnetic beads when driving the front end of the converter. Place a parallel capacitor or two single ended capacitors at the input to provide a matched passive network, and ultimately generate a low-pass filter at the input to filter out out out of band noise. The recommended input network is shown in Figures 10 and 11.

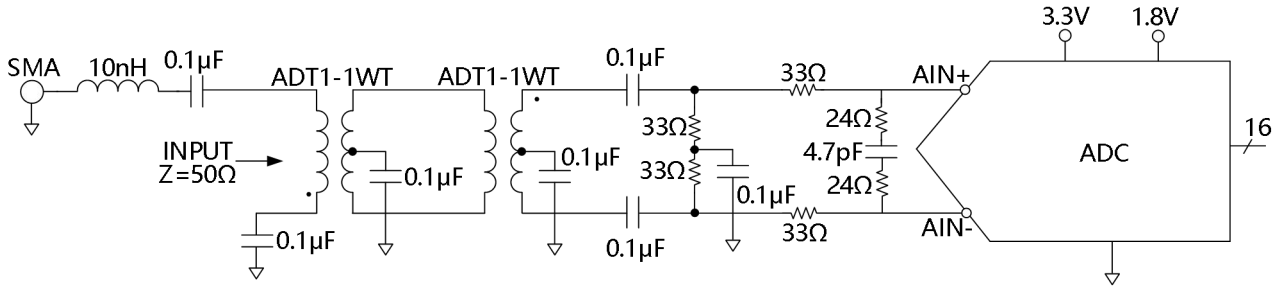


Figure 10. Low frequency input front-end network(~ 150MHz)

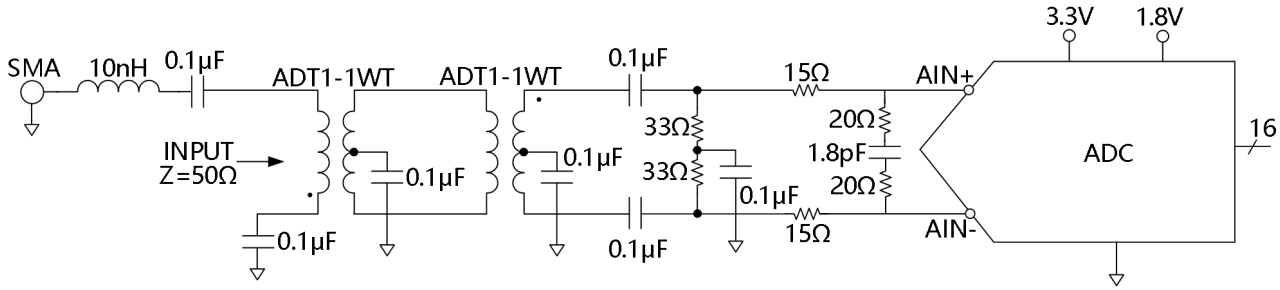


Figure 11. High frequency input front-end network (IF input 150MHz ~ 300MHz)

- **Timing specification**
  - **Clock input structure and recommended termination methods**

The ADC clock input structure is shown in Figure 12, which is a differential input structure and internally provides a 0.8V common mode voltage. The external clock should be excited using AC coupling. The recommended input structure of Barron is shown in Figure 13. The recommended input structure using LVPECL driver is shown in Figure 14. If using an LVDS driver, the recommended input structure is shown in Figure 15.

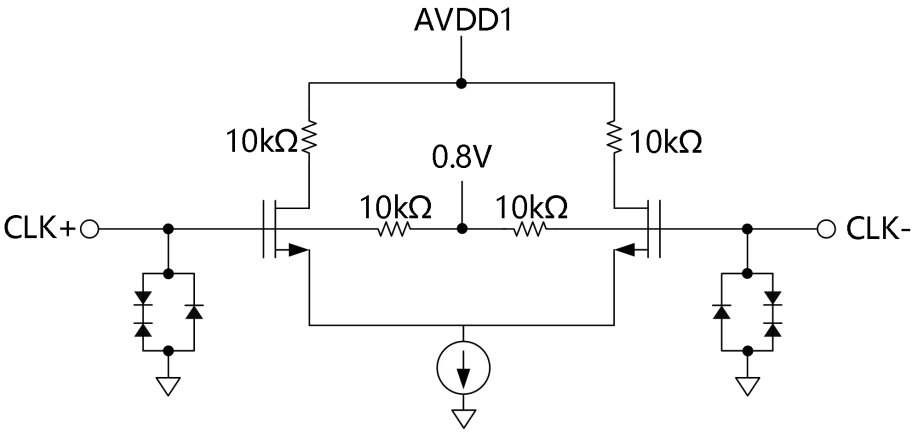


Figure 12. ADC clock input structure

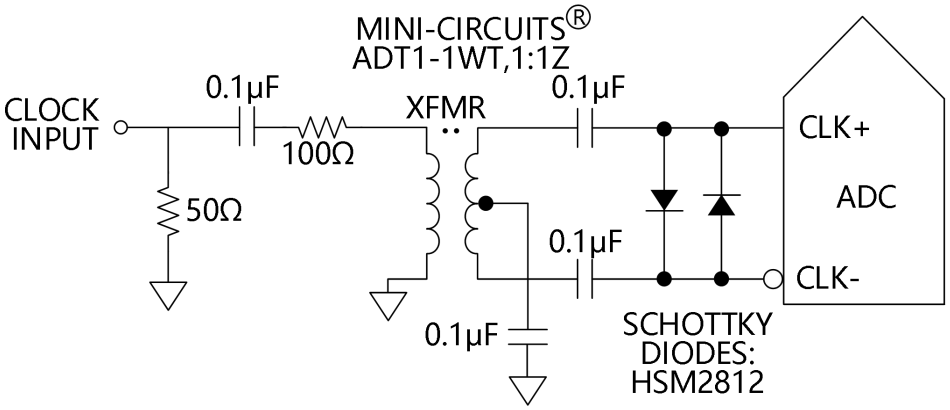


Figure 13. Clock Baron Excitation Scheme

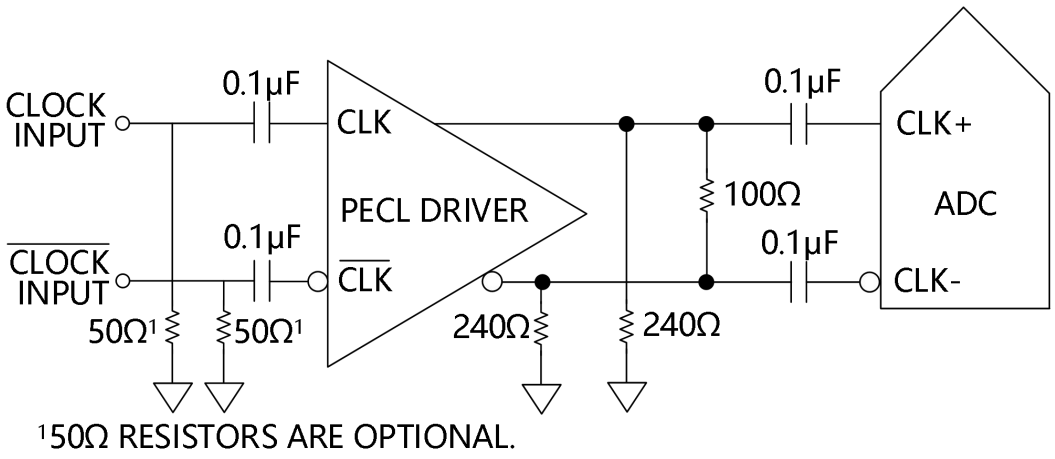


Figure 14. Clock LVPECL signal excitation scheme

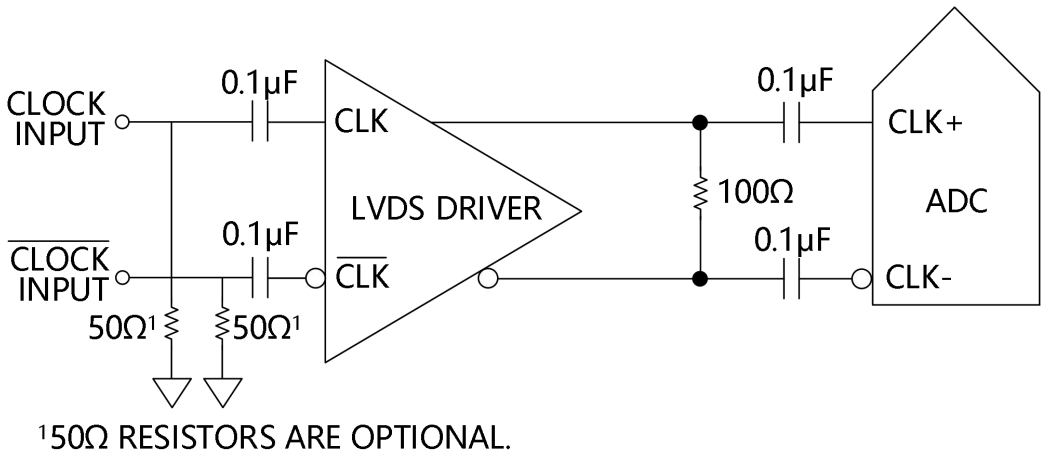


Figure 15. Clock LVDS signal excitation scheme

- **Clock level amplitude**

The minimum amplitude of the differential input clock signal is 250mVpp, compatible with LVDS/LVPECL levels, and the maximum allowable amplitude of a single end clock is VCM ± 0.9V. In order to reduce clock jitter and achieve optimal performance, it is advisable to provide clocks that rise and fall as quickly as possible. Increasing the signal amplitude under sine wave input can achieve the above effect. Under high-frequency input, it is recommended to increase the clock input amplitude as much as possible.

- **Duty cycle**

The ADC internal circuit uses the dual edges of the input clock to generate various timing signals. To ensure the chip's excellent performance, the input clock duty cycle should be ensured to be (50 ± 5)% during application.

- **Jitter**

High speed and high-precision ADC is very sensitive to clock jitter, especially when the input signal frequency is high. The relationship between signal-to-noise ratio (SNR) and jitter is $SNR=20\times lg(1/(2\pi\times f_{IN}\times t_{jitter}))$.To ensure the optimal SNR of this device under high-frequency analog input conditions, the system clock jitter is required to be less than 100fs.

- **Recommended clock design scheme**

The clock scheme adopts a single ended differential input, and it is recommended to use ADT1-1WT for transformers. The input and output are coupled with 0.1uF ceramic capacitors AC respectively. To obtain a symmetrical waveform, two back-to-back Schottky diodes can be connected in front of the ADC. When wiring a PCB, the differential clock wiring should be symmetrical and of equal length, and away from the analog input port. There should be some shielding between the clock and the analog input port (covered with copper on the ground). The recommended clock design scheme is shown in Figure 16.

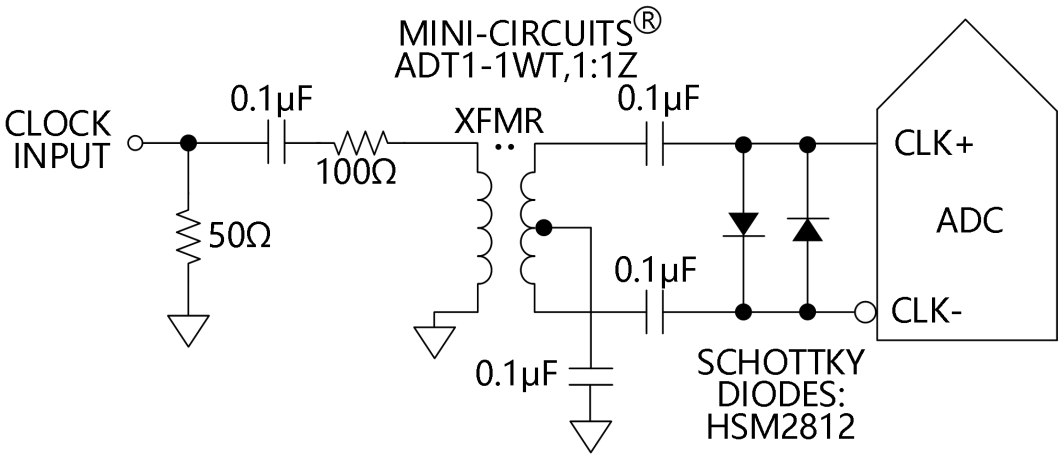


Figure 16. Recommended clock scheme

Notes

1. The heat sink pad should be in full contact with the ground and should be connected to the substrate of the PCB board through as many channels and sufficient area as possible.
2. The application circuit board has a complete and clean ground.
3. The application object is a multi-layer wiring board and contains independent layers.
4. Try to separate the digital ground and analog ground of the application object circuit board,and do not place the digital line next to the analog line or under the A/D converter.
5. The analog power supply and digital output power supply ports should be connected to high-quality ceramic bypass capacitors, and the bypass capacitors should be as close as possible to the pins. The shorter and wider the connection between the pins and the bypass capacitors, the better.
6. Differential inputs should be as close and parallel as possible.
7. The input wiring should be as short as possible to minimize parasitic capacitance and noise introduction.
8. All leads of the product are designed with electrostatic protection structures, but high energy electrical pulses may still damage the circuit. Therefore, attention should be paid to electrostatic protection during testing, handling, and storage.

Packaging and Outline Dimensions

QFN-72

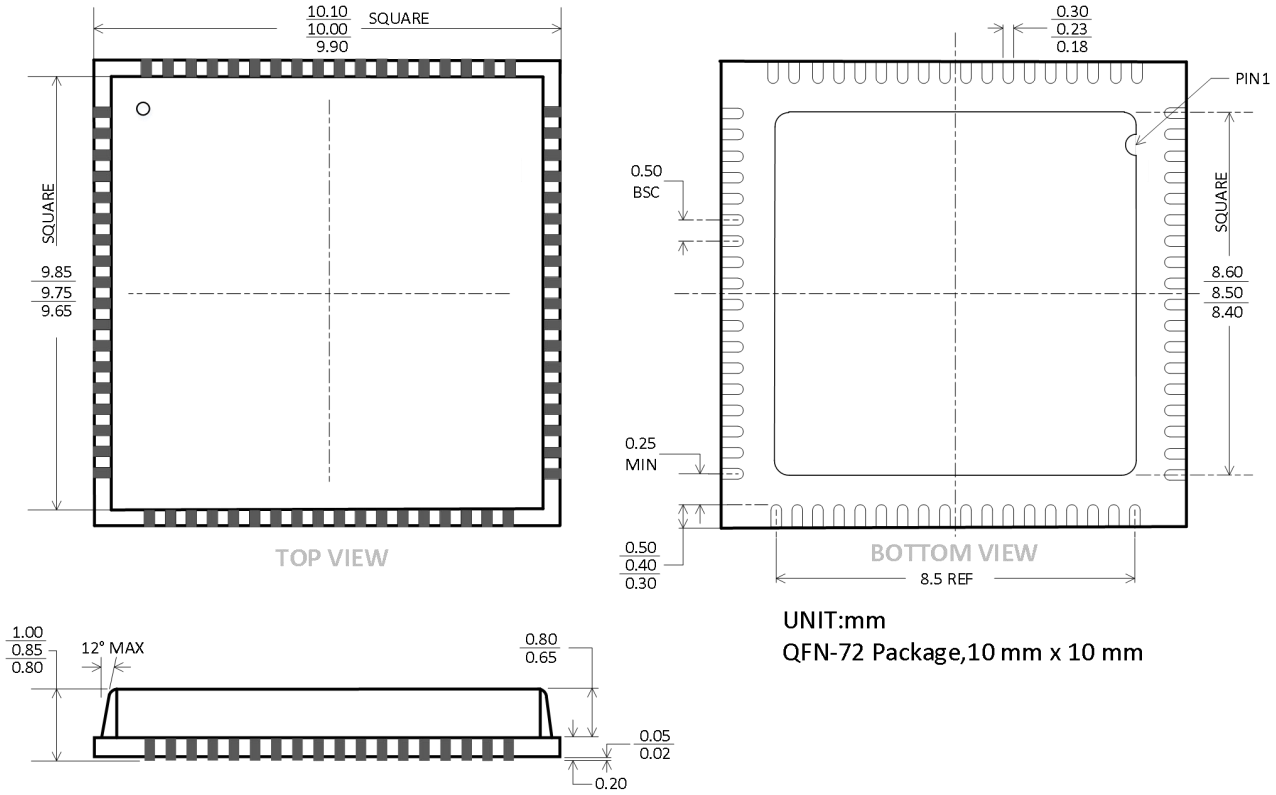


Figure 17. 72-Lead Outline Package [QFN]

Package/Ordering Informations

Product Name	Order code	temperature range	Product Packaging	Quantity	Packaging marking
CBM94AD67-200		-40℃+85℃	QFN-72	Tray,168	
CBM94AD67-250		-40℃+85℃	QFN-72	Tray,168	