Features

- Signal-to-Noise Ratio (SNR): 77 dBFS (at 9.7 MHz, VREF = 1.3 V)
- Signal-to-Noise Ratio (SNR): 75 dBFS (at 9.7 MHz, VREF = 1.0 V)
- Spurious-Free Dynamic Range (SFDR): 86 dBc (up to the Nyquist frequency, VREF = 1.3 V)
- Spurious-Free Dynamic Range (SFDR): 91 dBc (up to the Nyquist frequency, VREF = 1.0 V)
- Serial LVDS output
- Adjustable analog input range: 2.0 Vp-p / 2.6 Vp-p
- Powered by a 1.8 V power supply
- Low power consumption: Power consumption per channel ≤ 195 mW in 125 MHz mode
- Differential Nonlinearity (DNL): ±0.6 LSB
- Integral Nonlinearity (INL): ±5.0 LSB
- 650 MHz full-power analog input bandwidth
- Serial port control:
- Power-down mode for the whole chip and independent channels
- Built-in and user-defined test modes
- Multi-chip synchronization and clock division functions
- Standby mode

Application

- Medical Imaging
- High-speed Imaging
- Radio Receiver
- Portable Measuring Device

Description

This product is a 4-channel, 14-bit Analog-to-Digital Converter (ADC) with a sampling rate of 125 MSPS. It is specifically developed and designed for low power consumption, small size, and flexibility in use. The product can achieve a maximum conversion rate of 125 MSPS, boasting excellent dynamic performance and ultra-low power consumption, which makes it suitable for a wide range of application scenarios.

This ADC is powered by a single 1.8V power supply and accepts sampling clock signals compatible with LVPECL, CMOS, and LVDS. It can meet the requirements without the need for an external reference voltage source or driver.

It supports the function of independently turning off each internal channel. When all channels are disabled, the typical power consumption is less than 14 mW. This ADC is equipped with various built-in functions, such as programmable clock output, data alignment, and the generation of digital test codes. The available digital test codes include built-in fixed test codes and pseudo-random test codes. It also allows users to customize test codes via the Serial Port Interface (SPI).

This product comes in a 48-pin QFN48 package. The rated operating temperature range of this ADC is from -40°C to +85°C.

This product can be plug-and-play replaced with the AD9253 of Analog Devices, Inc. (ADI) in the United States.

Datalog

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Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.3.12			WW	LYL	Initial version generation
V1.1	2025.5.7	Update the error description of pin definition.	Error Update	WW	LYL	

Functional Block Diagram

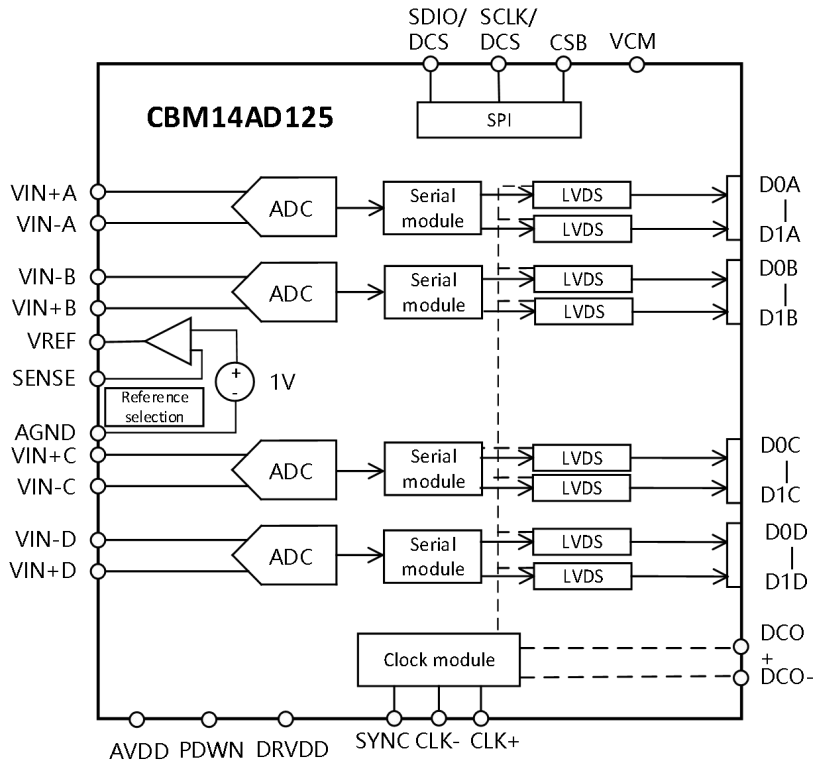

Figure 1. Functional Block Diagram

Pin configuration and functional description

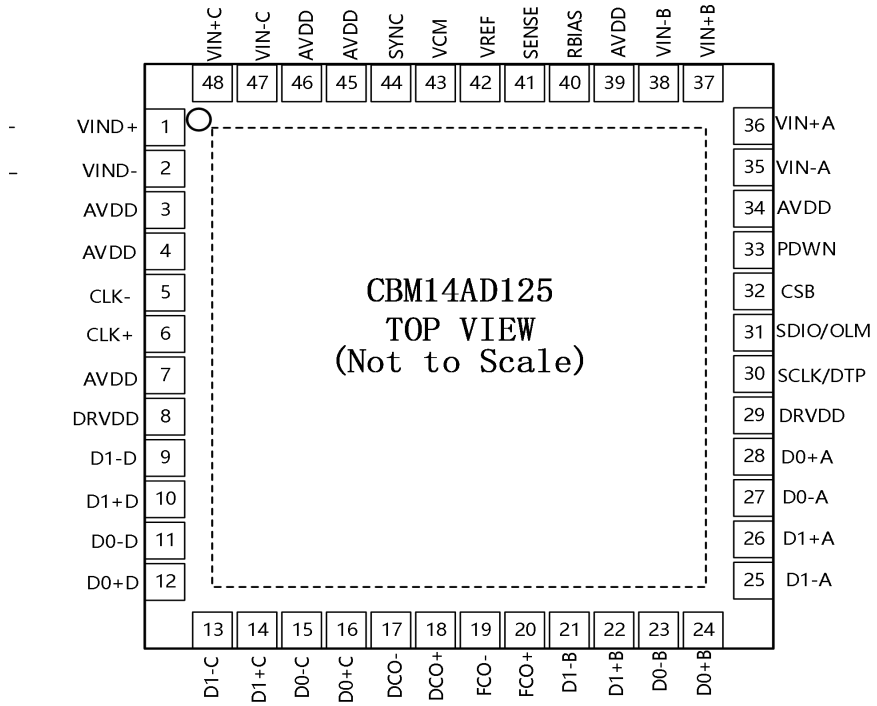

Figure 2. Pin Configuration

Pin NO.	Symbol	Pin Description
0	AGND	Analog ground
1	VIN+D	ADC analog input channel D+
2	VIN−D	ADC analog input channel D-
3,4,7,34,39, 45,46	AVDD	1.8 V analog power supply pin
5,6	CLK−, CLK+	Differential clock
8,29	DRVDD	Digital output drive power supply
9,10	D1−D, D1+D	The digital output of channel D
11,12	D0−D, D0+D	The digital output of channel D
13,14	D1−C, D1+C	The digital output of channel C

15,16	D0−C, D0+C	The digital output of channel C
17,18	DCO−, DCO+	Data clock output
19,20	FCO−, FCO+	Frame clock output
21,22	D1−B, D1+B	The digital output of channel B
23,24	D0−B, D0+B	The digital output of channel B
25,26	D1−A, D1+A	The digital output of channel A
27,28	D0−A, D0+A	The digital output of channel A
30	SCLK/DTP	SPI clock input/digital test mode.
31	SDIO/OLM	SPI data input and output
32	CSB	SPI Chip Select Signal
33	PDWN	Digital input (High level = Shutdown; Low level = Operation)
35	VIN-A	ADC analog input channel A-
36	VIN+A	ADC analog input channel A+
37	VIN+B	ADC analog input channel B+
38	VIN−B	ADC analog input channel B-
40	RBIAS	Set the analog current bias
41	SENSE	Reference voltage mode selection
42	VREF	Reference voltage input and output
43	VCM	Analog input common-mode voltage
44	SYNC	Digital input. Serves as the SYNC input of the clock divider.
47	VIN−C	ADC analog input channel C-
48	VIN+C	ADC analog input channel C+

Technical specifications

Electrical Characteristics

(Unless otherwise specified, VPP = 2.0V, VAVDD = VDRVDD = 1.8V, AGND = 0V, Fs = 125MSPS, and -40°C ≤ T_A ≤ 85°C.)

Parameters	Conditions	Min	Typ	Max	Unit
Resolution（RES)			14		位
Number of channels（N)			4		--
Offset Error (Eo)		-0.9	+0.3	-0.26	% FSR
Gain Error (Eg)		-14	+5	-4	% FSR
Differential Nonlinearity (DNL) (EDL)	f_{IN}=10MHz	-0.99	+1.5	±0.3	LSB
Integral Nonlinearity (INL) (EIL)	f_{IN}=10MHz	-10	+10	±2	LSB
Internal Reference Voltage Source (VREF)		0.95	1.05	1	V
Analog Input Common Mode Voltage Range (VCM)		0.8	1	0.9	V
Power Consumption (PW)		--	750	--	mW
Slew Rate (SR)		20	125	--	MSPS
Signal-to-Noise Ratio (SNR)		69	--	75.9	dBFS
Signal-to-Noise and Distortion Ratio (SINAD)		68	--	75.5	dBFS
Effective Number of Bits (ENOB)		11	--	12.1	bits
Spurious Free Dynamic Range (SFDR)		82	--	89	dBFS
Logic Input High Level (SCLK, SDIO, CSB)		1.2	1.8	--	V
Logic Input Low Level (SCLK, SDIO, CSB)		0	0.75	--	V

Switching Specifications

AVDD = 1.8 V, DRVDD = 1.8 V. Unless otherwise specified, AIN = -1.0 dBFS.

Parameters	Conditions	Min	Typ	Max	Unit
Clock Parameters					

Input Clock Rate	Full temperature range	20	--	1000	dBFs
Conversion Rate		20	--	125	dBFs
Clock High-Level Pulse Width (tEH)		--	4	--	dBFs
Clock Low-Level Pulse Width (tEL)		--	4	--	dBFs
Data Output Parameters					
Data Output Duty Cycle	Full temperature range	--	50	--	%
Wake-up Time	25℃	--	250	--	ns
Standby	25℃	--	375	--	μs
Pipeline Delay	25℃	--	16	--	Period
Transmission Delay	Full temperature range	--	2.3	--	ns
Output Rise Time	Full temperature range	--	300	--	ps
Output Fall Time	Full temperature range	--	300	--	ps
Aperture Parameters					
Aperture Delay (tA)	25℃	--	1	--	ns
Aperture Uncertainty (Jitter, tJ)	25℃	--	135	--	fs rms
Out-of-Range Recovery Time	25℃	--	1	--	Period

Timing Specifications

Parameters	Conditions	Limit value
SPI Timing Requirements		
t_{DS}	The setup time between the data and the rising edge of SCLK	2 ns,typ
t_{DH}	The hold time between the data and the rising edge of SCLK	2 ns,typ
t_{CLK}	SCLK period	40 ns,min
t_S	The setup time between CSB and SCLK	2 ns,min
t_H	The hold time between CSB and SCLK	2 ns,min
t_{HIGH}	SCLK high-level pulse width	10 ns,min
t_{LOW}	SCLK low-level pulse width	10 ns,min

t_{EN_SDIO}	The time required for the SDIO pin to switch from the input state to the output state relative to the falling edge of SCLK	10 ns,min
t_{DIS_SDIO}	The time required for the SDIO pin to switch from the output state to the input state relative to the rising edge of SCLK	10 ns,min

Timing Diagram

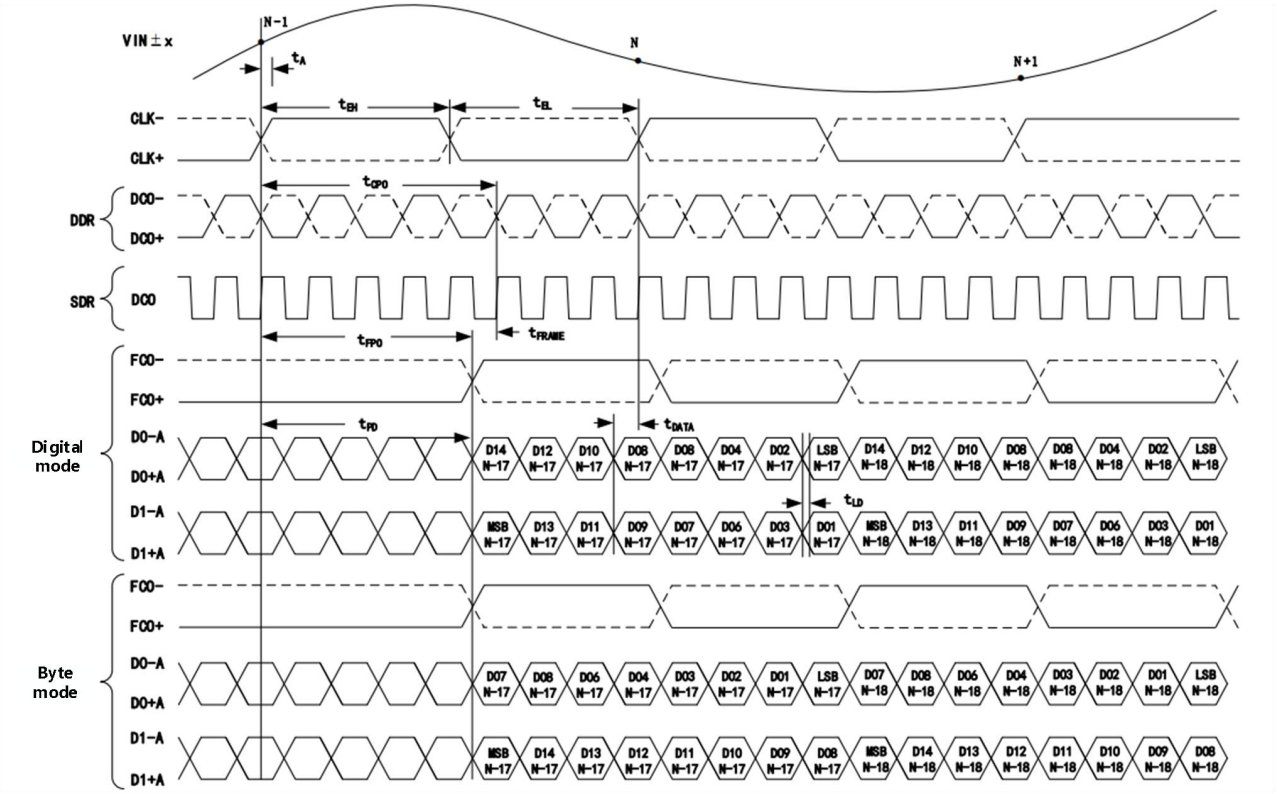

Figure 5. Data Output Timing

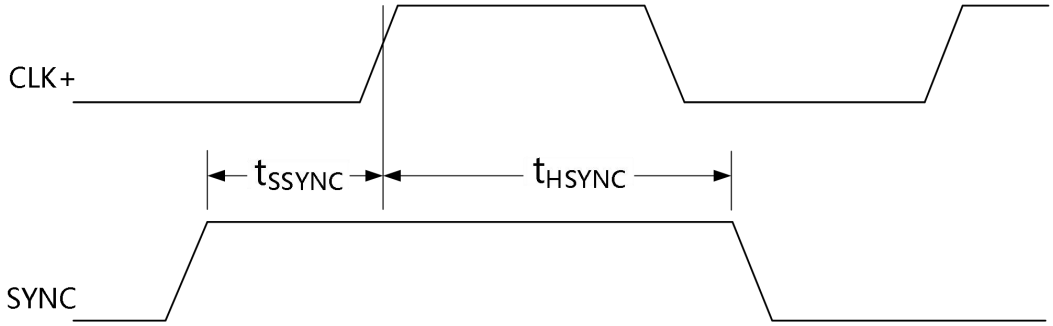

Figure 6. Timing Requirements for SYNC Input

Recommended operating conditions

- Operating frequency (fCLK): ≤125MHz
- Analog power supply voltage (AVDD): 1.75V~1.9V
- Digital power supply voltage (DVDD): 1.75V~1.9V
- Analog input common mode voltage (VCM): 0.5V~1.3V
- Operating ambient temperature (TA): −40°C to +85°C
- Input signal amplitude range (peak-to-peak): (VIN(P-P)) ≤2V

Absolute maximum rating

Parameters	Range
Analog power supply voltage (VAVDD)	2V
Digital power supply voltage (VDRVDD) 2V	2V
Junction temperature	150℃
Storage temperature range	-65℃ to 150℃

Typical Performance

Unless otherwise specified, the test conditions are as follows: AVDD = 1.8V, DRVDD = 1.8V, SVDD = 1.8V, the sampling rate is 125MSPS, the differential input is 2Vp-p, VIN = -1dBfs, and T_A = 25℃.

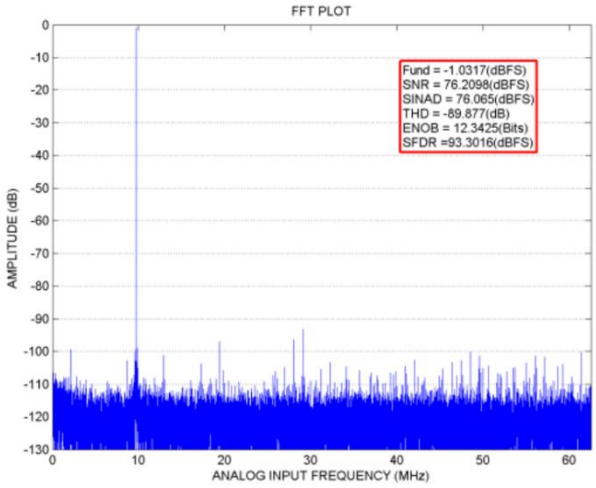

Figure 7. Single tone 32K(f_{IN}=10MHz，fS=125MSPS)

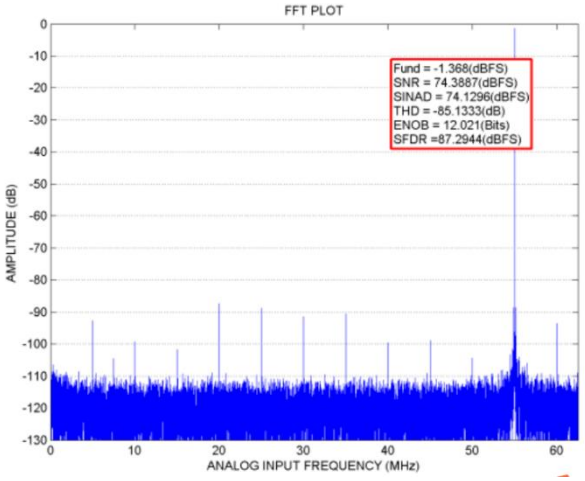

Figure 8. Single tone 32K(f_{IN}=70MHz，f_S=125MSPS)

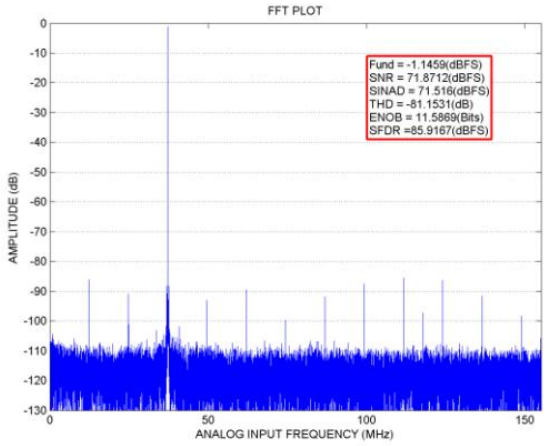

Figure 9. Single tone 32K(f_{IN}=140MHz，f_S=125MSPS)

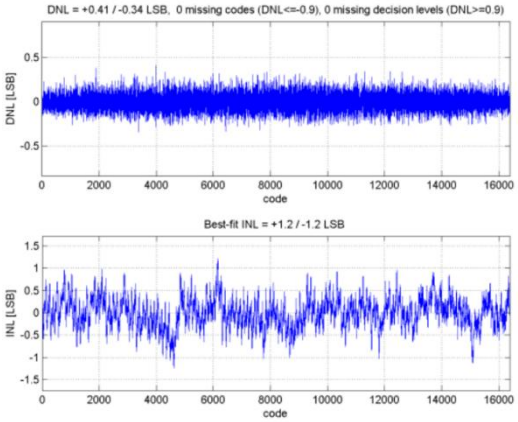

Figure 10. DNL/INL(f_{IN}=10MHz，f_S=125MSPS)

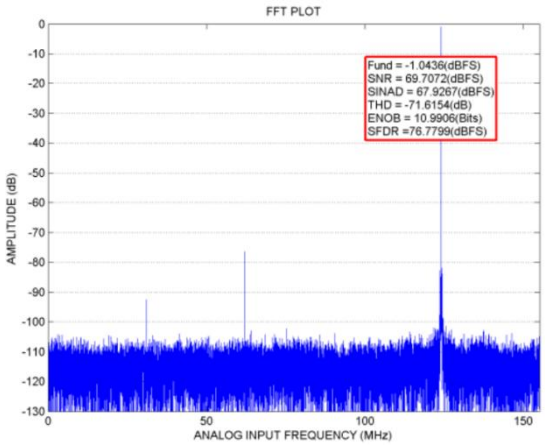

Figure 11. SFDR、SNR VS input frequency

Equivalent circuit

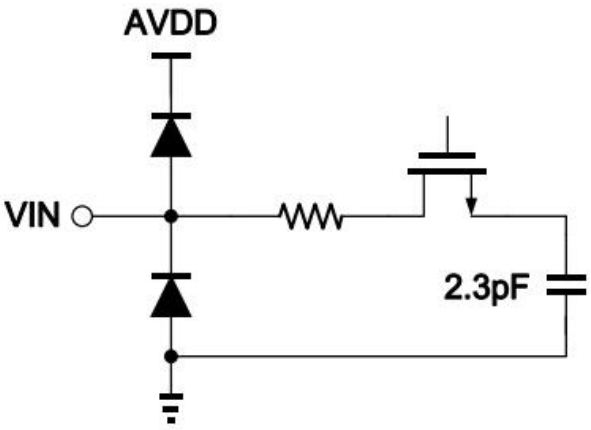

Figure 12 Equivalent Analog Input Circuit

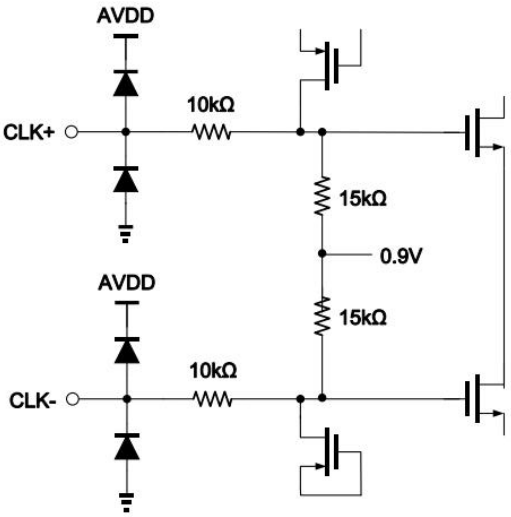

Figure 13 Equivalent Clock Input Circuit

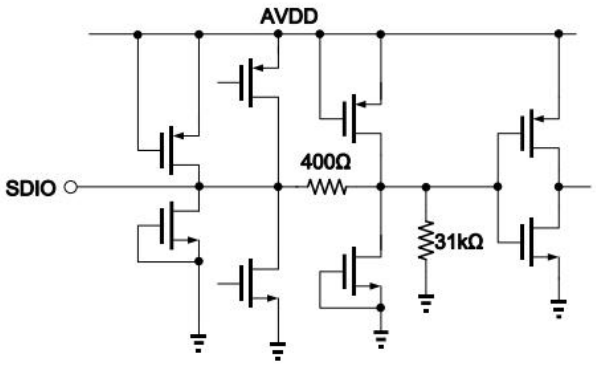

Figure 14 Equivalent SDIO Input Circuit

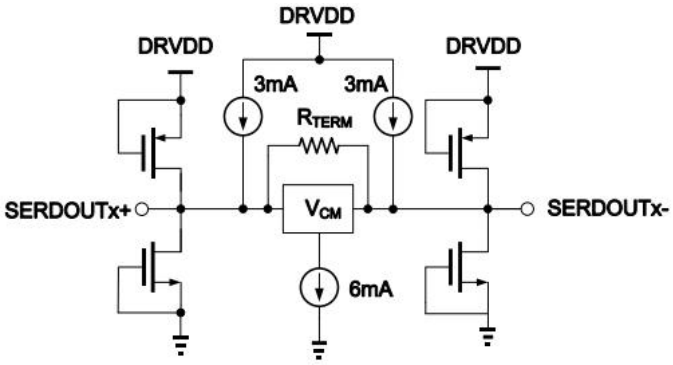

Figure 15 Equivalent SERDOUT± Circuit

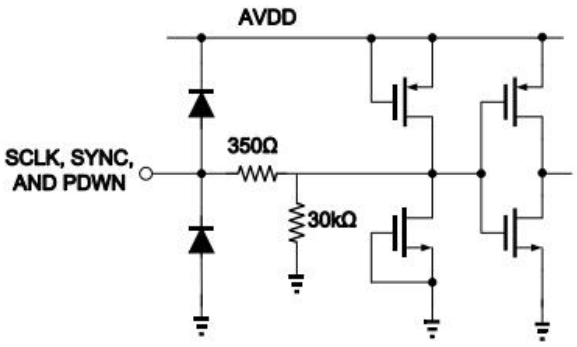

Figure 16 Equivalent SCLK, SYNC, PDWN Circuit

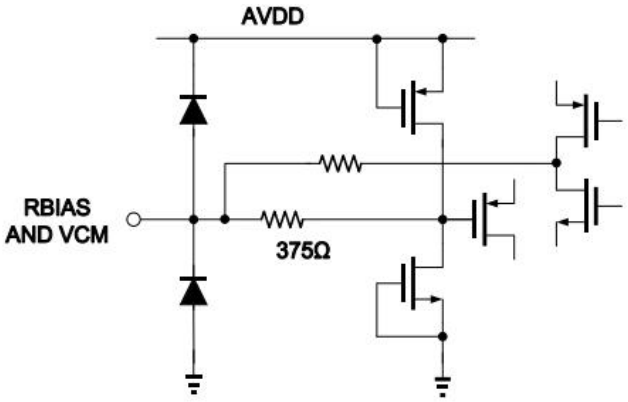

Figure 17 Equivalent RBIAS, VCM Circuit

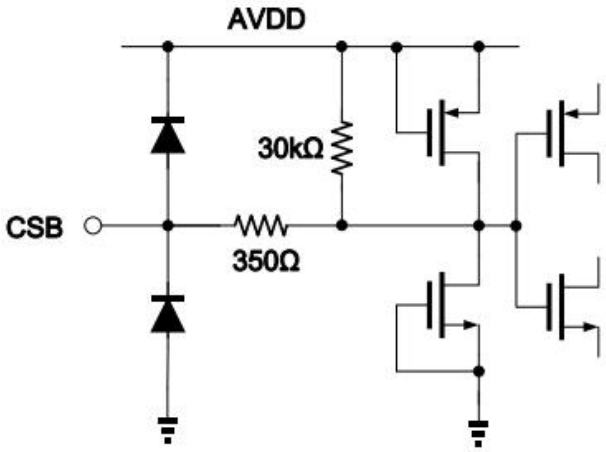

Figure 18 Equivalent CSB Input Circuit

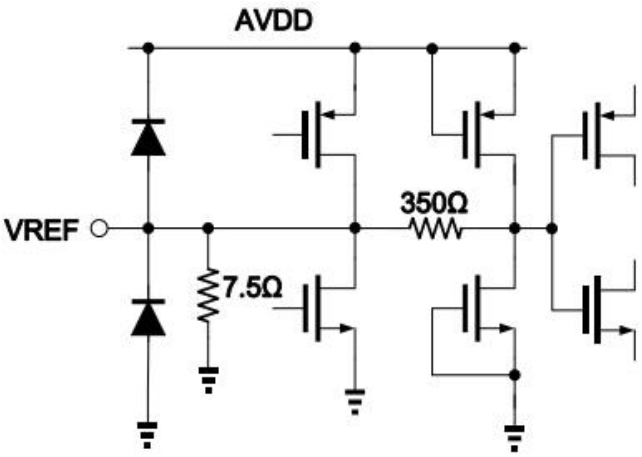

Figure 19 Equivalent VREF Circuit

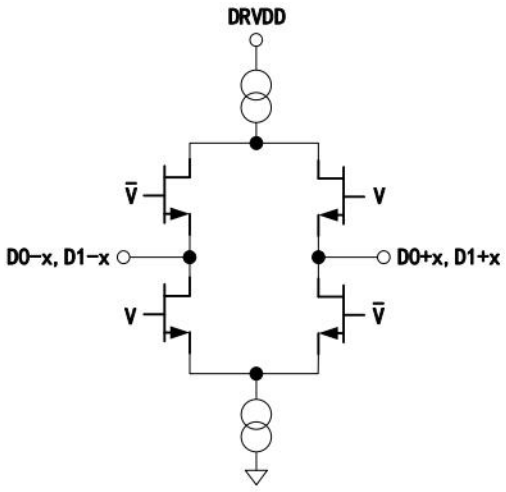

Figure 20 Equivalent Output Circuit

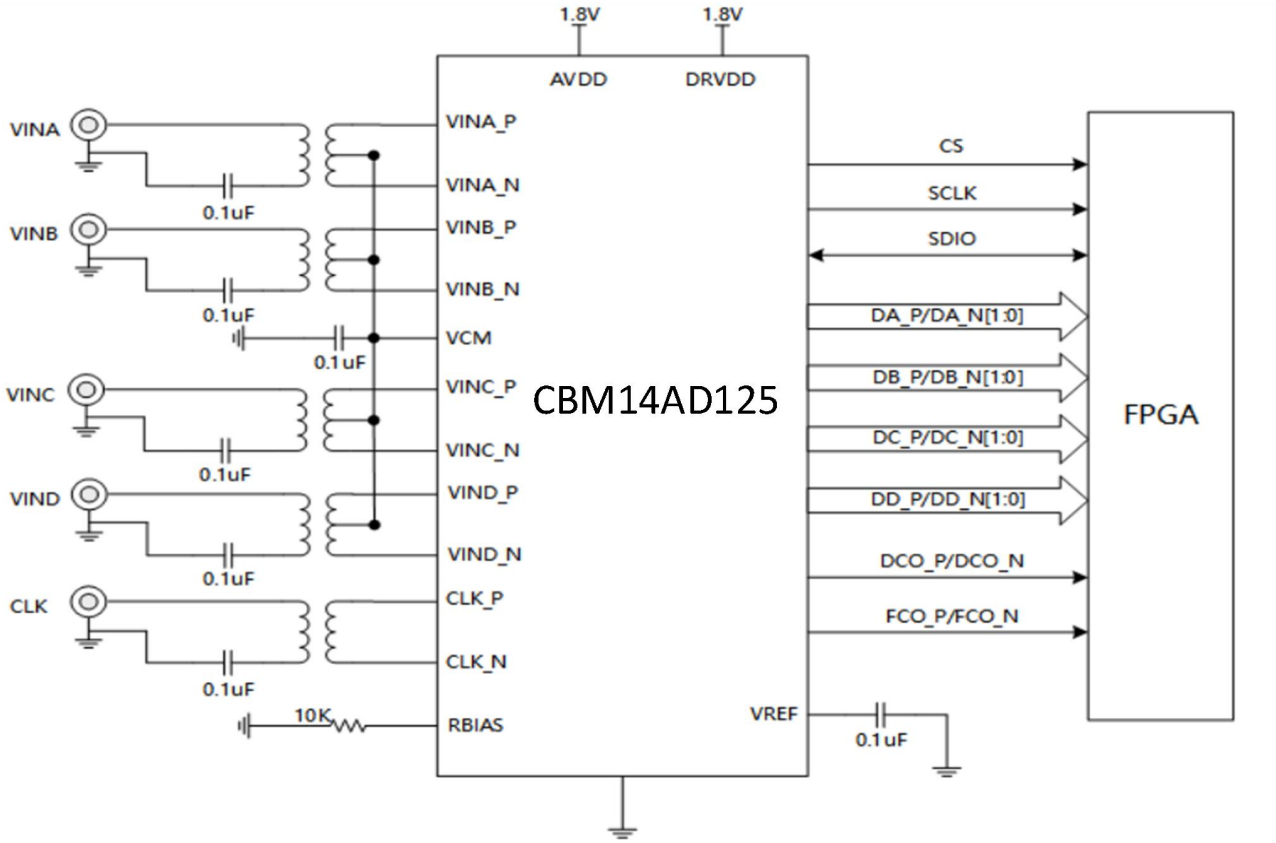

Figure 21 Typical Application Circuit of CBM14AD125 (2Vpp Mode)

Operating principle

The core of this product uses a multi-stage pipelined ADC architecture. Each stage provides one redundant bit to eliminate the offset error of the coarse quantization comparator. The quantization structure of each stage of the pipeline is reconstructed by a shift adder in the digital domain to form a 14-bit conversion result. The serializer sends this conversion result in a 14-bit output format. Except for the last stage, each stage of the pipeline consists of a low-resolution Flash ADC, a switched capacitor DAC connected to it, and an inter-stage residue amplifier (such as a multiplying digital-to-analog converter [MDAC]). The residue amplifier amplifies the difference between the output of the reconstruction DAC and the input of the Flash ADC to provide it to the next stage of the pipeline. To assist in the digital correction of Flash errors, each stage is set with a redundancy of one bit. The last stage consists only of a Flash ADC.

Analog Input Terminal

The analog input terminal of this product is a differential switched capacitor circuit designed to handle differential input signals. This circuit supports a wide common-mode range while maintaining excellent performance. When the input common-mode voltage is the intermediate

power supply voltage, the signal-related errors are minimized, and the best performance can be achieved.

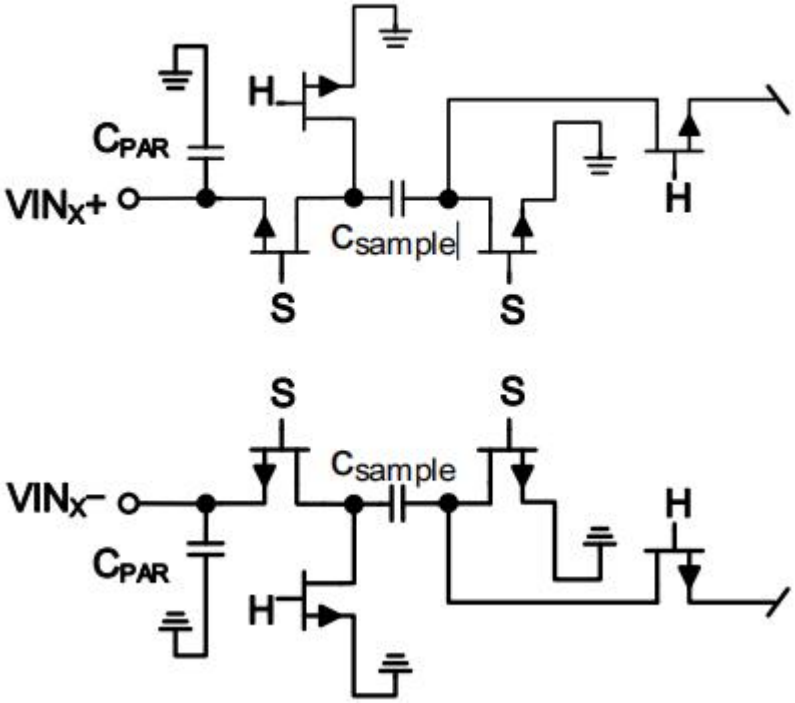

Figure 22 Switched Capacitor Input Circuit

The input circuit switches between the sampling mode and the holding mode according to the clock signal (see Figure 22). When the input circuit switches to the sampling mode, the signal source must be capable of charging the sampling capacitor and completing the establishment within half a clock cycle. A small resistor is connected in series at each input terminal to help reduce the peak transient current injected from the output stage of the driving source. In addition, a low-Q inductor or a ferrite bead can be used on each side of the input terminal to reduce the high differential capacitance at the analog input terminal, thereby achieving the maximum bandwidth of the ADC. When driving the front end of the converter at high and intermediate frequencies (IF), a low-Q inductor or a ferrite bead must be used. A differential capacitor or two single-ended capacitors can be used at the input terminal to provide a matched passive network. This will ultimately form a low-pass filter at the input terminal to limit unwanted broadband noise.

Input Common Mode Level

The analog input terminal of this product has no internal DC bias. In AC-coupled applications, the user must provide an external bias. To obtain the best dynamic performance, the user must configure the device so that the input common mode level

VCM = AVDD/2. This product provides an on-chip reference voltage through the VCM pin, and a 0.1 μF capacitor must be used to bypass the VCM pin to the ground. In the differential configuration, setting the device input to the maximum range can achieve the highest signal-to-noise ratio (SNR) performance. For this product, the input range depends on the reference voltage, and the performance will deteriorate sharply if it exceeds the input range.

Differential Input Configuration

There are various active and passive methods to effectively drive this product. Driving it in a differential manner can suppress even-order harmonics and thus obtain the best performance.

In baseband applications, driving this product with a differential balun configuration can provide excellent performance and a flexible interface for the ADC (refer to Figure 23).

In applications where SNR is a critical parameter, since the noise performance of most amplifiers is insufficient to meet the actual performance of this product, the input configuration requires differential transformer coupling (refer to Figure 24).

The value selection of capacitor C1 in the above two applications needs to be coordinated with the input spectrum. It is recommended to reduce the capacitance value of this capacitor or remove it when converting high-frequency analog input signals.

It is not recommended to drive this product in a single-ended input mode.

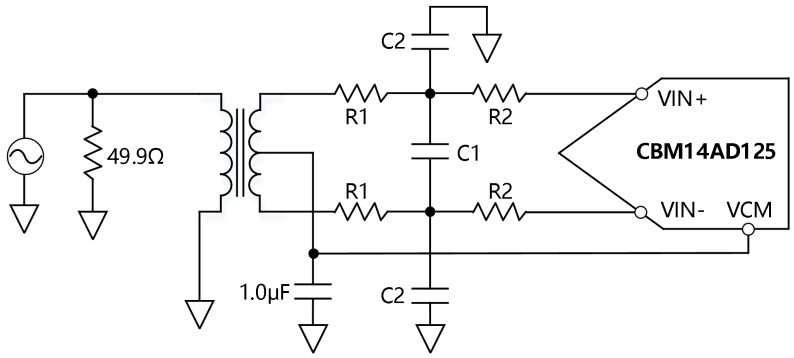

Figure 23. Differential Transformer Coupling Input Configuration

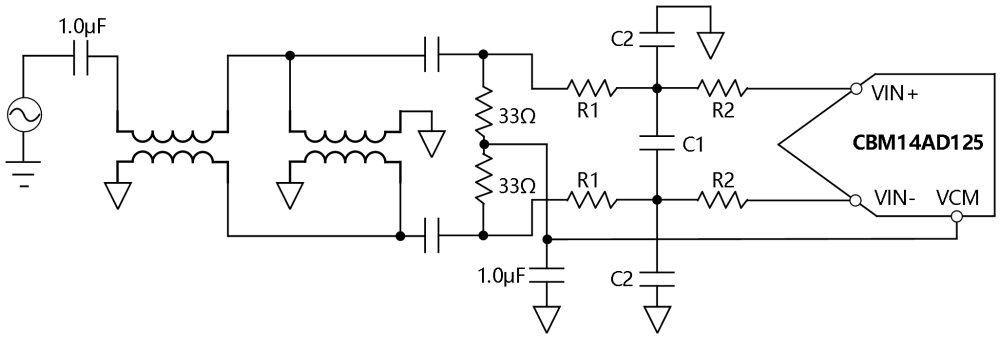

Figure 24. Differential Dual Balun Coupling Input Configuration

RC Network Example

Frequency Range (MHz)	Series Resistance R1 (Ω)	Differential Capacitance C1 (pF)	Series Resistance R2 (Ω)	Shunt Capacitance C2 (pF)
0 to 100	10~33	5	15	15
100 to 300	10	5	10	10

Reference Voltage Connection

This product has a built-in stable and accurate reference voltage source. VREF can be configured using the internal 1.0 V reference voltage, an externally applied reference voltage ranging from 1.0 V to 1.3 V, or an external resistive voltage divider acting on the internal reference voltage, generating a user-selectable reference voltage. For the description of the reference voltage source mode, please refer to the "Internal Reference Voltage Connection" section and the "External Reference Voltage" section. The VREF pin should be bypassed to ground in parallel through an external 1.0 μF capacitor with a low equivalent series resistance (ESR) and a 0.1 μF ceramic capacitor with a low ESR.

The built-in comparator of this product can detect the voltage of the SENSE pin, thereby configuring the reference voltage into one of three possible modes. If the SENSE pin is grounded, the reference voltage amplifier switch is connected to the internal resistive voltage divider (see Figure 25), thus setting the voltage V of the VREF pin to 1.0 V. If the SENSE pin is connected to an external resistive voltage divider (see Figure 26), then VREF is defined as: VREF = 0.5 x (1 + R2/R1), where 7 kΩ ≤ (R1 + R2) ≤ 10 kΩ.

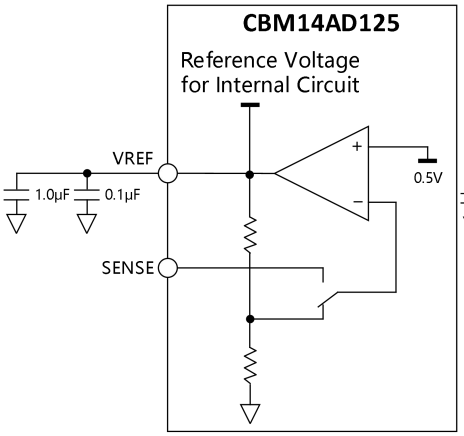

Figure 25. SENSE Pin Grounded Mode
(VREF Internal Configuration Mode)

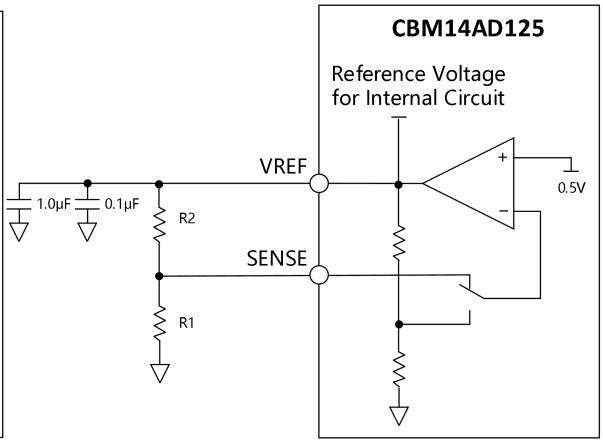

Figure 26. External Resistor String Mode
(VREF External Configuration Mode)

If you want to use the internal reference voltage of this product to drive multiple converters, so as to improve the matching degree of the gain, the load of the reference voltage imposed by other converters must be taken into account. Figures 27 and 28 show how the load affects the internal reference voltage.

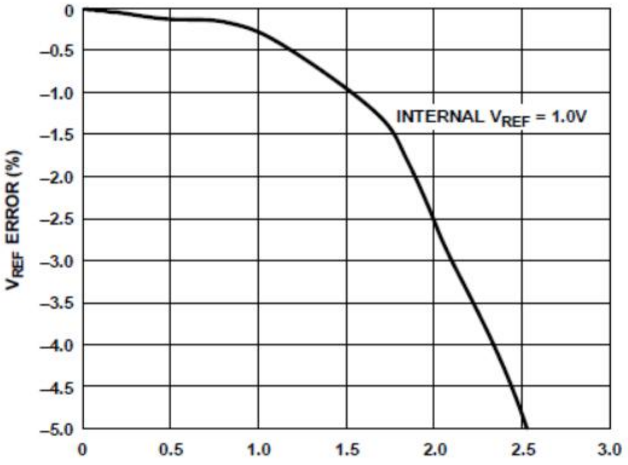

Figure 27 VREF error(internal VREF = 1.0 V)VS load current

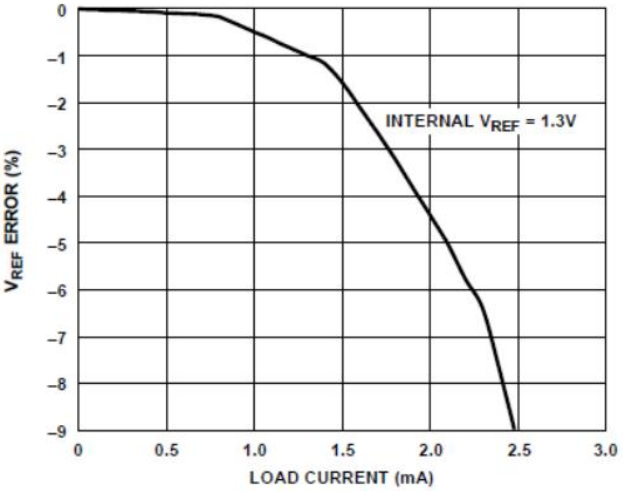

Figure 28 VREF error(internal VREF = 1.3 V)VS load current

- **External Reference Voltage**

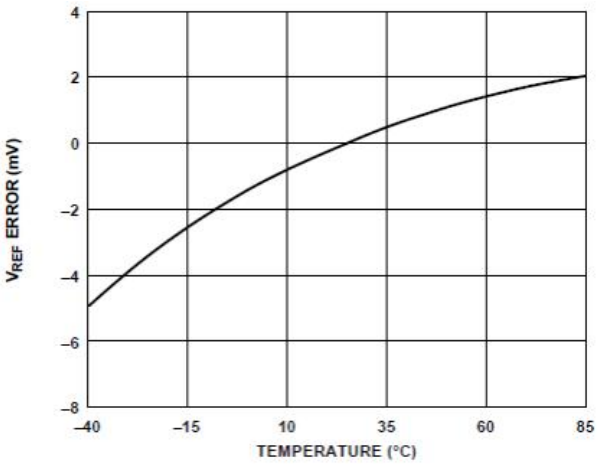

Figure 29 VREF error VS temperature (VREF = 1.0 V typical drift of VREF = 1.0 V)

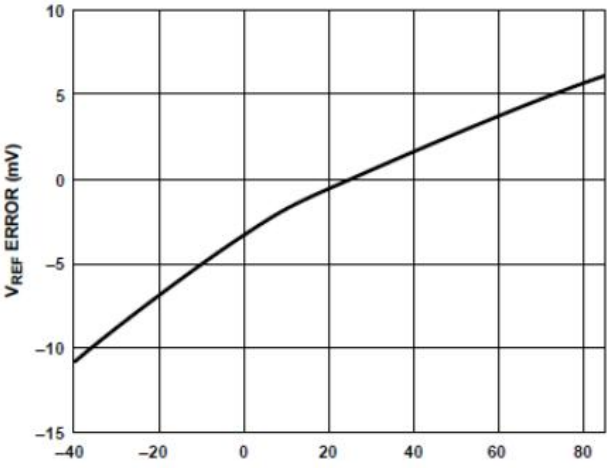

Figure 30 VREF error VS temperature (VREF = 1.0 V typical drift of VREF = 1.3 V)

An external reference voltage must be used to further improve the ADC gain accuracy and the thermal drift characteristics. Figures 29 and 30 show the typical drift characteristics of the internal reference voltage source in the 1.0 V mode and 1.3 V mode respectively. When the SENSE pin is connected to AVDD, the internal reference voltage source can be disabled, allowing the use of an external reference voltage source. The load of the internal reference voltage buffer

on the external reference voltage source is equivalent to a 7.5 kΩ load. The internal buffer generates positive and negative full-scale reference voltages for the ADC core. It is not recommended to leave the SENSE pin floating.

Clock Input Considerations

To fully utilize the performance of the chip, a differential signal should be used as the clock signal for the sampling clock input terminals (CLK+ and CLK−) of this product. This signal is usually AC-coupled to the CLK+ and CLK− pins using a transformer or a capacitor. These two pins have internal bias and do not require external bias.

Clock Input Options

This product has a flexible clock input structure. CMOS, LVDS, LVPECL or sinusoidal signals can all be used as its clock input signals. Regardless of the type of signal used, the clock source jitter must be taken into account (see the description in the jitter considerations section). A single-ended signal from a low-jitter clock source can be converted into a differential signal using a RF transformer or a RF balun. For clock frequencies ranging from 125 MHz to 1 GHz, a RF balun configuration is recommended; for clock frequencies ranging from 40 MHz to 200 MHz, a RF transformer configuration is recommended. Schottky diodes connected across the secondary winding of the transformer/balun can limit the clock signal input to this product to approximately 0.8 V differential peak-to-peak (see Figures 31 and 32). In this way, it can prevent the large voltage swing of the clock from feeding through to other parts of the product, and it can also preserve the fast rise and fall times of the signal, which is very important for achieving low jitter performance. However, when the frequency is higher than 500 MHz, the capacitance of the diodes will have an impact. Care must be taken to select appropriate signal limiting diodes.

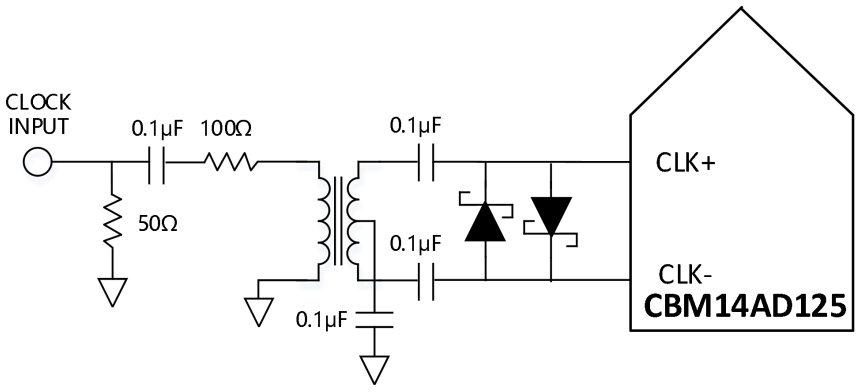

Figure 31.Clock Input with Transformer Configuration

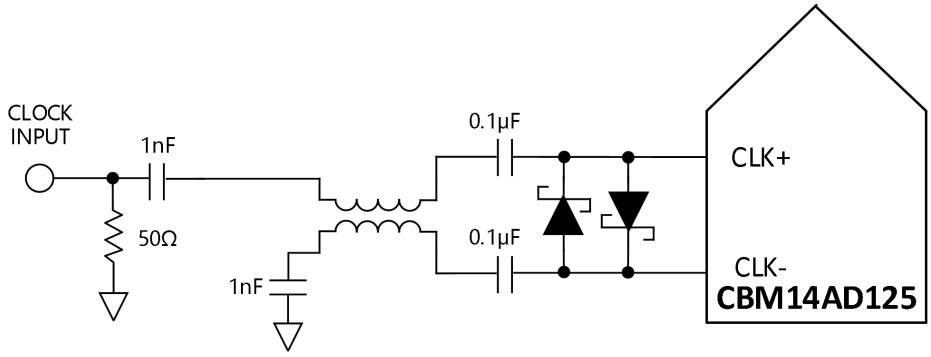

Figure 32.Clock with Balun Configuration

If there is no low-jitter clock source, then another approach is to AC-couple the differential PECL signal and transmit it to the sampling clock input pins (as shown in Figure 33). The AD951X clock drivers have excellent jitter performance.

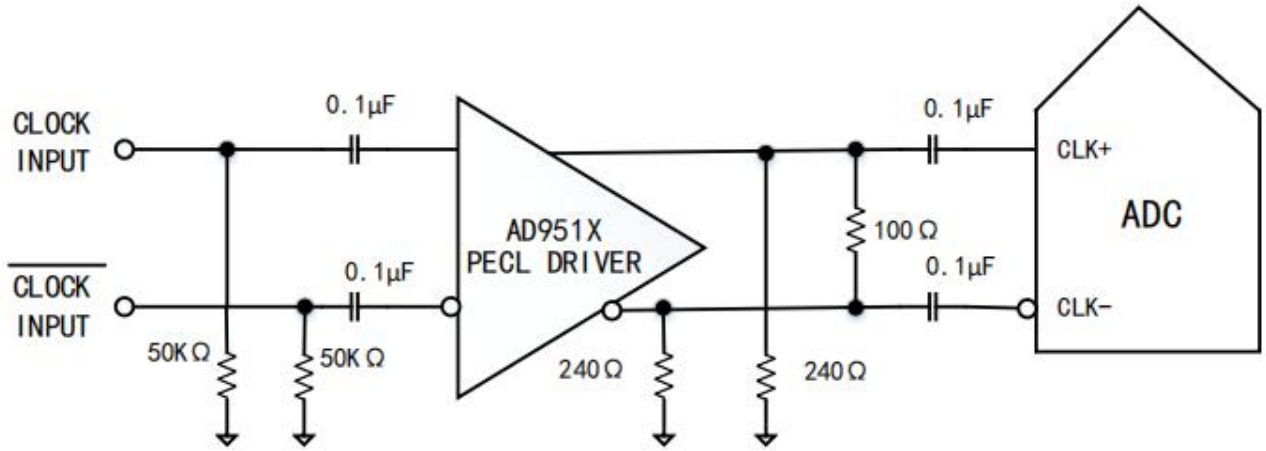

Figure 33 Differential PECL sampling clock (the frequency can reach up to 1 GHz)

Another method is to AC-couple the differential LVDS signal to the sampling clock input pins (as shown in Figure 34). The AD951X clock driver has excellent jitter performance.

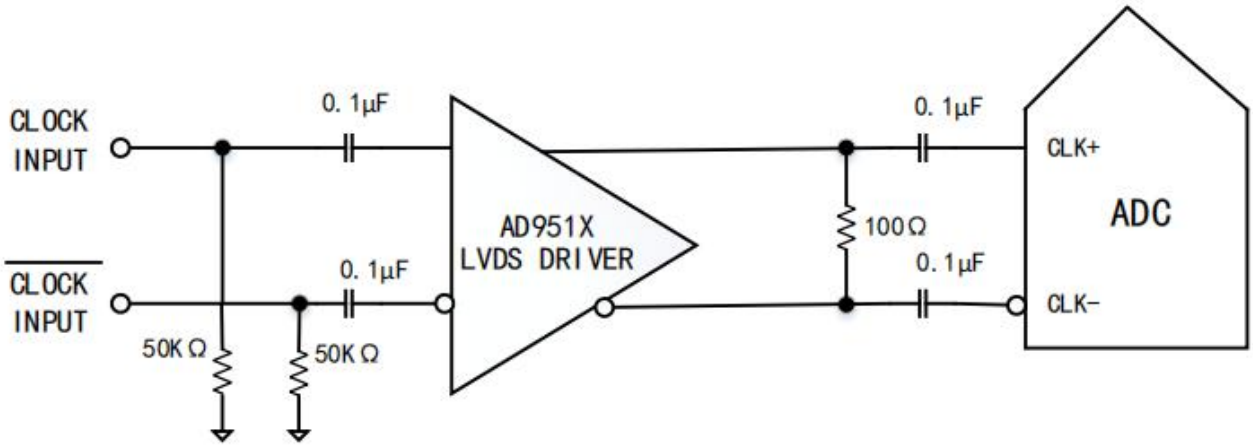

Figure 34 Single-ended 1.8 V CMOS input clock (with a frequency of up to 200 MHz)

Input Clock Divider

This product has a built-in input clock divider that can divide the input clock by an integer multiple ranging from 1 to 8. The clock divider of this product can be synchronized by using an external SYNC input signal. By writing to bits 0 and 1 of register 0x109, it is possible to set whether the clock divider is resynchronized each time the SYNC signal is received or only after the first receipt of the SYNC signal. A valid SYNC can reset the divider to its initial state. This synchronization feature can align the clock dividers of multiple devices, thereby ensuring simultaneous input sampling.

Clock Duty Cycle

Typical high-speed ADCs use two clock edges to generate different internal timing signals, so they are very sensitive to the clock duty cycle. Generally, to maintain the dynamic performance of the ADC, the clock duty cycle tolerance should be ±5%. This product has a built-in duty cycle stabilizer (DCS) that can retime the non-sampling edge (falling edge) and provide an internal clock signal with a nominal duty cycle of 50%. When the clock input duty cycle deviates from the nominal 50% duty cycle by more than the ±5% rated value, this feature can minimize the performance degradation. Enabling the DCS function can significantly improve the noise and distortion performance for clock input duty cycles in the ranges of 30% to 45% and 55% to 70%. The jitter of the input rising edge still deserves attention, and this jitter cannot be easily reduced with the help of the internal stabilizing circuit. In applications where the clock rate changes dynamically, the time constant associated with this loop must be considered. It is necessary to wait for a period of 1.5 μs to 5 μs before the DCS loop relocks to the input signal.

Jitter Considerations

High-speed and high-resolution ADCs are very sensitive to the quality of the clock input signal. Intermediate frequency undersampling applications are particularly sensitive to jitter (see Figure 35).

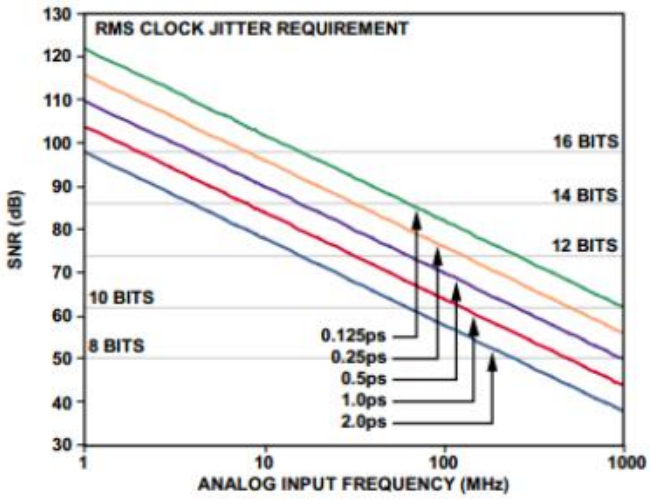

Figure 35 The relationship between the ideal signal-to-noise ratio and the analog input frequency and jitter.

When the aperture jitter may affect the dynamic range of this product, the clock input signal should be regarded as an analog signal. Separate the power supply of the clock driver from that of the ADC output driver to prevent digital noise from being mixed into the clock signal. A crystal-controlled oscillator with low jitter can provide the best clock source. If the clock signal comes from other types of clock sources (through gating, frequency division or other methods), it is necessary to use the original clock for retiming in the last step.

Power Consumption and Power Saving Mode

As shown in Figure 36, the power consumption of this product is proportional to its sampling rate. This product can be put into the power saving mode through the SPI port or by setting the PDWN pin high. In the power saving mode, the typical power consumption of the ADC is 2 mW. In the power saving mode, the output driver is in a high-impedance state. When the PDWN pin is set low, this product returns to the normal operating mode. Note that PDWN is referenced to the power supply voltage (DRVDD) of the data output driver and must not be higher than this power supply voltage. In the power saving mode, low power consumption is achieved by turning off the reference voltage source, the reference voltage buffer, the bias network, and the clock. When entering the power saving mode, the internal capacitors are discharged; when returning to the normal operating mode, the internal capacitors must be recharged. Therefore, the wake-up time is related to the time in the power saving mode; the shorter the time in the power saving mode, the shorter the corresponding wake-up time. When using the SPI port interface, the user can place the ADC in the power saving mode or the standby mode. For a shorter wake-up time, the standby

mode can be used, in which the internal reference voltage circuit is powered on. For more information on using these functions, please refer to the "Memory Map" section.

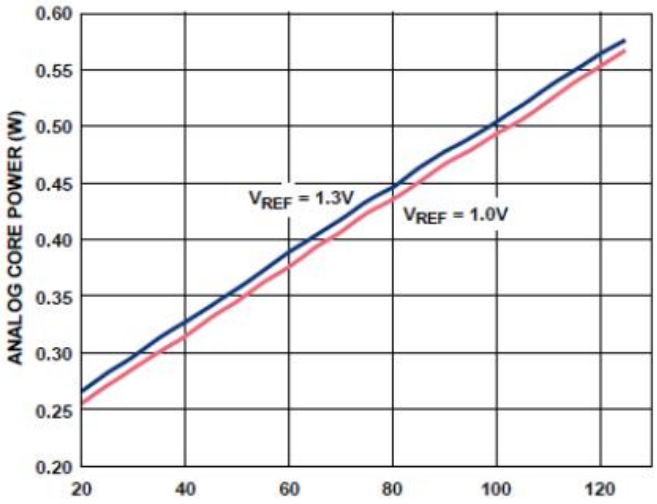

Figure 36 Total Power Consumption VS f_{SAMPLE}

Digital Output

The digital output of this product complies with the ANSI-644 LVDS standard. The output current is 3.5 mA, with a terminating resistor of 100 ohms as the load and a swing of 350 mV. In the default mode, the timing relationship of the output is shown in Figure 37.

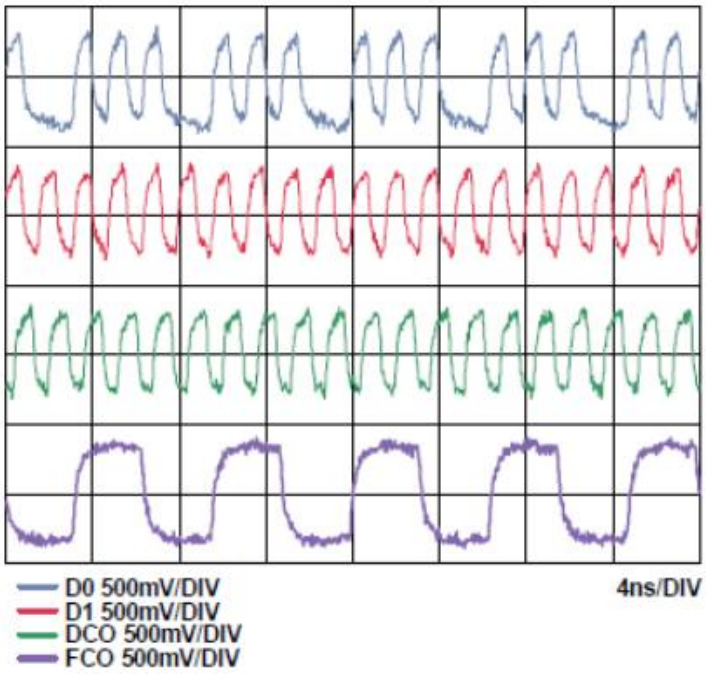

Figure 37 Example of LVDS Output Timing Sequence

SPI Control

The SPI of this product adopts a three-wire control mode. The timing control diagram of the SPI is shown in Figure 38.

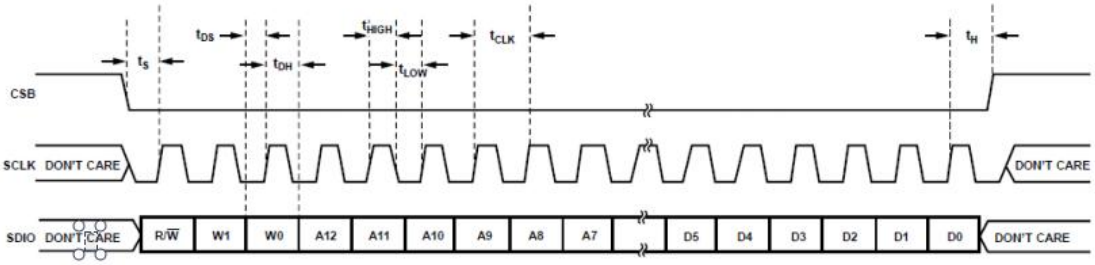

Figure 38 SPI Timing

Register List

Address	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default (Hex)	Note
0x00	Spi configuration(global)	0=SDOvalid	LSBpriority	Soft Reset	1=16-bit address	1=bit address	Soft Reset	LSB priority	0=SDOvalid	0x18	R/W
0x01	Chip ID(global)	8bit Chip ID [7:0] 0xB5 = Quad channels、14 bit、125 MSPS serial LVDS								0xB5	R
0x02	Chip Level(global)	disable	Speed levelID[6:4] 110=125MSPS			disable	disable	disable	disable		R
Device Index and Transfer Register											
0x05	Device Index	disable	disable	Clock ChannelDCO	Clock ChannelFCO	Clock Channel D	Clock ChannelC	Clock ChannelB	Clock ChannelA	0x3F	R/W
0xFF	Transfer Register	disable	disable	disable	disable	disable	disable	disable	Start overlay	0x00	W
globalADC Functional Register											
0x08	Power Consumption Mode(global)	disable	disable	Function of the external power-down pin:	disable	disable	disable	Internal setting of the power consumption mode: 00 = Normal operation 01 = Complete power down 10 = Standby 11 = Reset		0x00	R/W

				0 = Power down 1 = Standby							
0x09	Clock(global)	disable	disable	disable	disable	disable	disable	disable	Clock Duty Cycle Stability Enable: 0 = On 1 = Off	0x01	R/W
0x0B	Clock Frequency Division (global)	disable	disable	disable	disable	disable	Clock frequency division ratio: 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8			0x00	R/W
0x0C	disable	disable	disable	disable	disable	disable	Chopping Mode 0 = Off 1 = On	disable	disable	0x00	R/W
0x0D	Test mode (local)	User Input Test Mode 00 = Single 01 = Alternate 10 = Single Once 11 = Alternate Once (Only affects the user input test mode, bits [3:0] = 1000)		Reset PN Long Sequence	Reset PN Short Sequence	disable	Output Test Mode [3:0] (local) 0000 = Off (default) 0001 = Intermediate Level Short Sequence 0010 = Positive FS 0011 = Negative FS 0100 = Alternating Checkerboard Pattern 0101 = PN 23 Sequence 0110 = PN 9 Sequence 0111 = 1/0 Word Inversion 1000 = User Input 1001 = 1/0 Bit Inversion 1010 = 1× Synchronization 1011 = 1 Bit High Level 1100 = Mixed Bit Frequency			0x00	R/W
0x10	Offset adjustment (local)	8-bit device offset adjustment, bits [7:0] (local) The offset adjustment is in units of LSB, ranging from +127 to -128 (in two's complement format).								0x00	R/W

0x14	Output Mode	disable	LVDS ANSI/ LVDS-IEEE Options 0 = LVDS ANSI 1 = LVDS IEEE Narrow the scope Link (global);	disable	disable	disable	Output Inversion (local):	disable	Output Format 0 = Offset Binary 1 = Two's Complement Binary (global)	0x01	R/W
0x15	Output Adjustment	disable	disable	Output Driver Side Connection [1:0] 00 = None 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω		disable	disable	disable	Output Drive 0 = 1× Drive 1 = 2× Drive	0x00	R/W
0x16	Output Phase	disable	Input Clock Phase Adjustment [6:4] (The value represents the number of input clock cycles of the phase delay)			Output Clock Phase Adjustment [3:0] (Ranging from 0000 to 1011)				0x03	R/W
0x18	VREF select (global)	disable	disable	disable	disable	disable	VREF Regulation Digital Scheme [2:0] 000 = 1.0 V p-p (1.3 V p-p) 001 = 1.14 V p-p (1.48 V p-p) 010 = 1.33 V p-p (1.73 V p-p) 011 = 1.6 V p-p (2.08 V p-p) 100 = 2.0 V p-p (2.6 V p-p)			0x04	R/W
0x19	USER_PATT1_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	
0x1A	USER_PATT1_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B0	0x00	
0x1B	USER_PATT2_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	

0x1C	USER_PATT2_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B0	0x00	
0x21	Serial Output Data Control (global)	LVDS Output LSB priority	SDR/DDR Single Channel/Dual Channel, Bit-by-Bit/Byte-by-Byte [6:4] 000 = SDR Dual Channel, Bit-by-Bit 001 = SDR Dual Channel, Byte-by-Byte 010 = DDR Dual Channel, Bit-by-Bit 011 = DDR Dual Channel, Byte-by-Byte 100 = DDR Single Channel, Word-by-Word			disable	Select 2× Frame	Number of Serial Output Bits 00 = 16 位		0x30	
0x22	Serial Channel Status (Local)	disable	disable	disable	disable	disable	disable	Channel Output Reset	Channel Power-down	0x00	
0x100	Sampling Rate Coverage	disable	Sampling Rate Coverageable	Always write =01		disable	Sample rate 000 = 20 MSPS 001 = 40 MSPS 010 = 50 MSPS 011 = 65 MSPS 100 = 80 MSPS 101 = 105 MSPS 110 = 125 MSPS			0x00	
0x101	User I/O Control 2	disable	disable	disable	disable	disable	disable	disable	SDIO Pull down	0x00	
0x102	User I/O Control 3	disable	disable	disable	disable	VCM Power-down	disable	disable	disable	0x00	VCM Control。
0x106	Comparator Threshold algorithm	reserve						00 = Off 01 = Turn on Level 1 10 = Turn on Level 2 11 = Turn on Level 1/2		0x00	

0x109	Synchronization	disable	disable	disable	disable	disable	disable	Only synchronize with the next synchronization pulse.	Enable Synchronization	0x00	

Package Outline and Dimensions

QFN-48

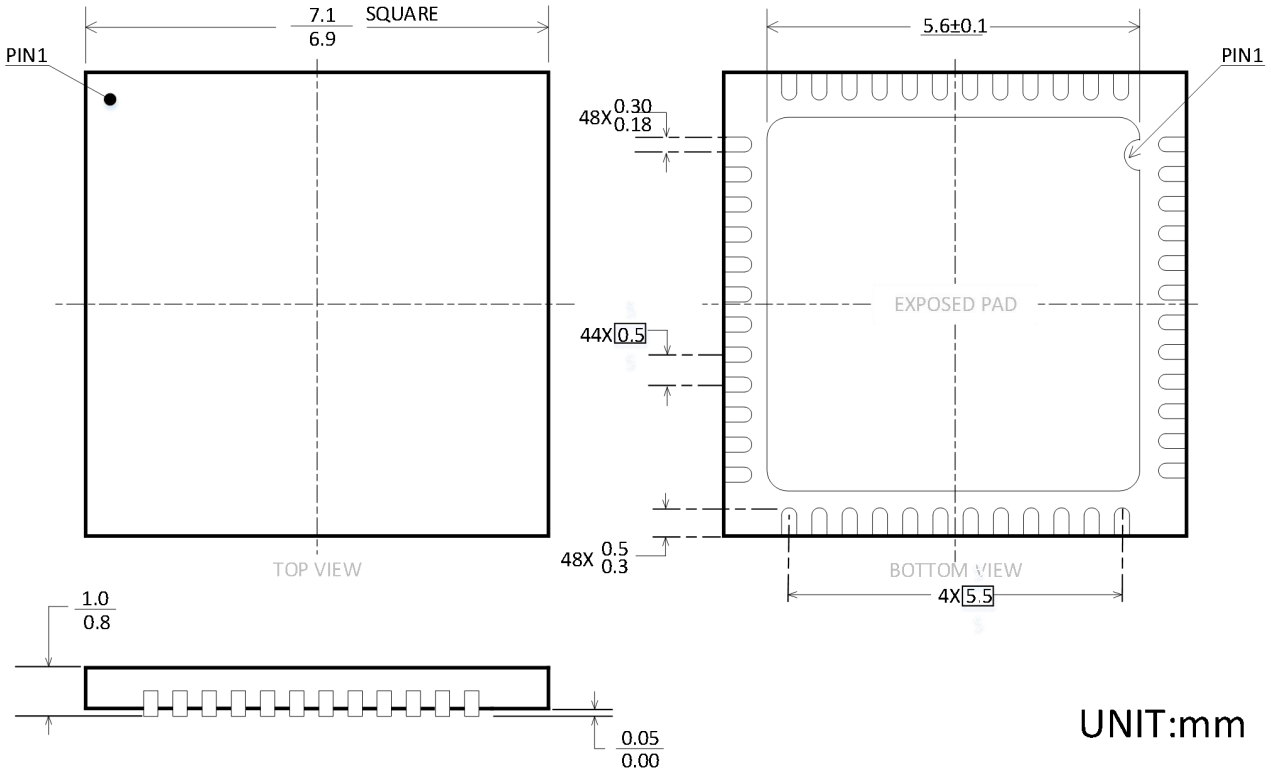

Figure39. Dimension Diagram of QFN-48 Package

Packaging/Ordering Information

PRODUCT TYPE	Order Code	OPERATING TEMPERATURE	PACKAGE	PACKAGE MARKING	NUMBER OF PACKAGES
CBM14AD125		-40℃~85℃	QFN-64	Tray，250	