Features

- **Dual transmitters**
- **Dual receivers**
- **Dual input observation receivers**
- **Maximum receiver bandwidth 200MHz**
- **Maximum transmitter bandwidth 450MHz**
- **Maximum observation receiver bandwidth 450 MHz**
- **Integrated fractional-N frequency synthesizers**
- **Integrated clock synthesizer**
- **Multichip phase synchronization for RF LO and baseband clocks**
- **JESD204B interface 12.288Gbps lane rate**
- **Tuning range (center frequency) 75 MHz to 6000 MHz**
- **Each Rx/Tx can operate at different frequencies**
- **Zero-IF or Low-IF operation**

Applications

- Radar system4G/5G microcell base stations
- Active antenna systems
- Massive multiple input/output(MIMO)
- Phased array radar
- Test equipment

General Description

The CBMRF9009 is a highly integrated, radio frequency (RF), agile transceiver offering dual transmitters and receivers, integrated synthesizers, and digital signal processing functions.

The receive path consists of two independent direct conversion receivers with 200MHz receiver bandwidth.

CBMRF9009 also supports two observation path receivers (ORX) that can be used for digital predistortion (DPD) function.

The complete receive subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, thus eliminating the need for these functions in the digital baseband.

The received signals are digitized with a set of interleaved pipeline ADCs that provide inherent antialiasing. The combination of the direct conversion architecture, which does not suffer from out of band image mixing, and the lack of aliasing, eases the requirements of the RF filters when compared to traditional intermediate frequency (IF) receivers.

The transmitters use a direct conversion modulator that achieves high modulation accuracy with exceptionally low noise.

The observation receiver path includes manual attenuation control, dc offset correction, quadrature error correction and digital filtering, thus supporting wide receiver bandwidth and high dynamic range.

The observation receive path supports 450MHz receive bandwidth, and can be used as wide bandwidth receiver without automatic gain control (AGC) function.

The high speed JESD204B interface supports up to 12.28Gbps lane rates, and can be configured for receive data and transmitter data flexibly.

The power supplies of CBMRF9009 include 1.0V, 1.2V, 1.8V and 3.3V.These voltages can be generated form linear regulators or switching regulators.

CBMRF9009 uses an SPI interface to communicate with the external processor.

CBMRF9009 is packaged in a 12mm x 12mm, 196-ball Flip chip ball grid array (CSP BGA).

CBMRF9009 supports an operating temperature range of -40~+85℃.

Datalog

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Revision History

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.8.20					
V1.1	2025.11.26	Deletion of frequency conversion modes and correction of receiver bandwidth errors	Error Update	WW	LYL	

Functional Block Diagram

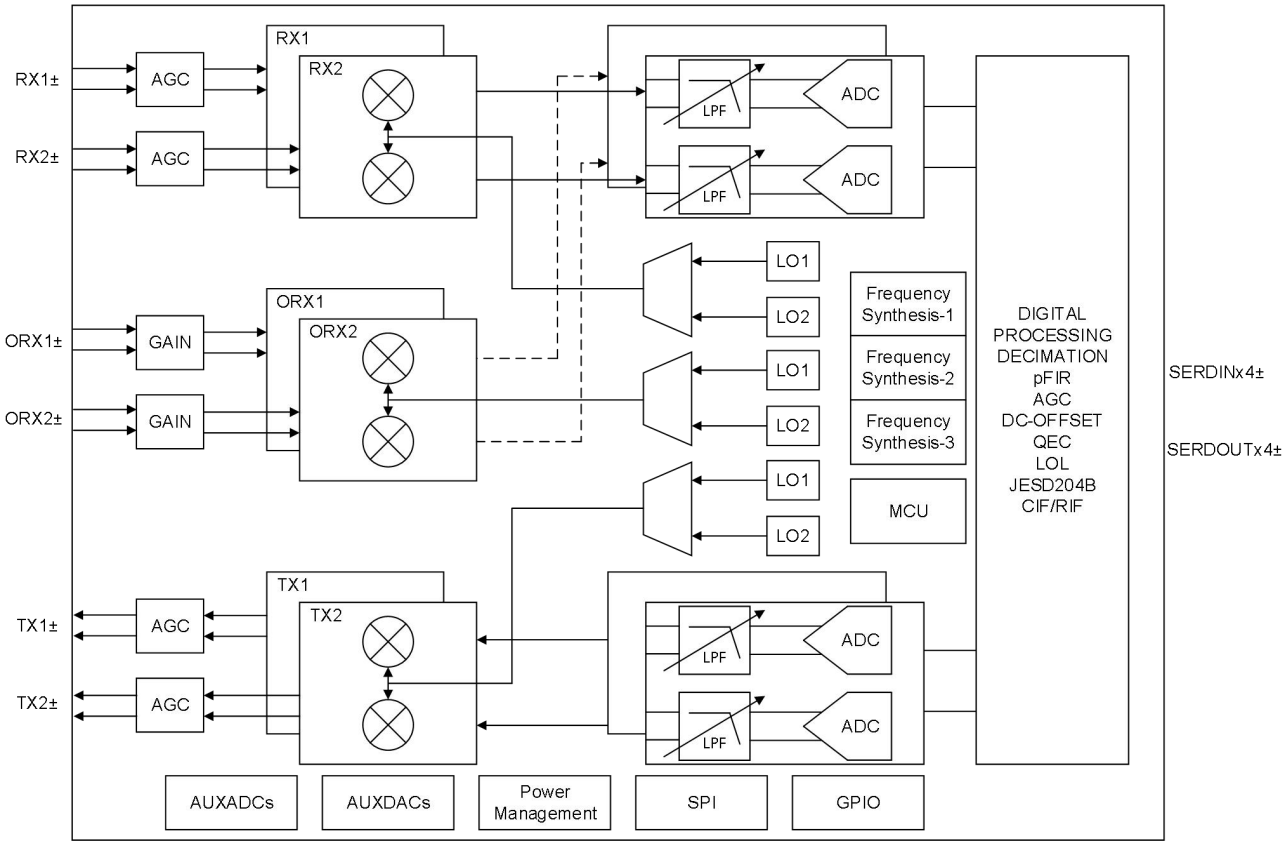

Figure 1 Functional Block Diagram

Specifications

Electrical characteristics at VDDA1P2 = 1.2V, VDDD1P0_DIG = 1.0V, VDDA1P8_TX = 1.8V, Local oscillator frequency = 1800MHz, unless otherwise noted. Receiver and transmitter path loss is shown in Table 1 and Table 2.

Table 1

Frequency	TX path loss
0.1GHz~5GHz	2dB
5GHz~5.5GHz	3dB
5.5GHz~6GHz	3.5dB

Table 2

Frequency	TX path loss
0.1GHz~3GHz	2dB
3GHz~4GHz	2.5dB
4GHz~5.5GHz	3dB
5.5GHz~6GHz	3.5dB

Operation configuration:

RX BW 200MHz (IQ rate = 245.76MHz), analog gain 0dB;
TX BW 450MHz (IQ rate = 491.52MHz), analog attenuation 0dB;
ORX BW 450MHz (IQ rate = 491.52MHz), analog attenuation 0dB;
Reference clock frequency = 122.88MHz.

Table 3

TRANSMITTERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
Frequency range		75		6000	MHz	
Transmitter band width				450	MHz	
Transmitter pass band flatness		±1			dB	
Transmitter attenuation		0		31.5	dB	
Transmitter attenuation step			0.5		dB	
Adjacent Channel Leakage Ratio	ACPR					100MHz bandwidth OFDM
			-57		dB	LO=0.7GHz, -13dBFs
			-55		dB	LO=2.595GHz, -12dBFs
			-53		dB	LO=4.88GHz, -15dBFs
In Band Noise Floor						Test at LO+50MHz
			-143.2		dBm/Hz	LO=75MHz
			-143.6		dBm/Hz	LO=300MHz
			-145.8		dBm/Hz	LO=700MHz
			-147.2		dBm/Hz	LO=1800MHz
			-148.2		dBm/Hz	LO=2600MHz
			-149.3		dBm/Hz	LO=3600MHz
			-149.4		dBm/Hz	LO=4600MHz
			-149.7		dBm/Hz	LO=5500MHz
			-149.3		dBm/Hz	LO=5800MHz
Interpolation Images			-80		dBc	
TX1 to TX2 Isolation			97		dB	LO=300MHz

			99		dB	LO=700MHz
			91		dB	LO=1800MHz
			75		dB	LO=2600MHz
			77		dB	LO=3600MHz
			85		dB	LO=4600MHz
			78		dB	LO=5500MHz
			69		dB	LO=5800MHz
Image Rejection Ratio	IRR					20MHz offset from LO
			59		dBc	LO=300MHz
			63		dBc	LO=700MHz
			62		dBc	LO=1800MHz
			65		dBc	LO=2600MHz
			65		dBc	LO=3600MHz
			62		dBc	LO=4600MHz
			57		dBc	LO=5500MHz
			58		dBc	LO=5800MHz
Maximum Output Power						Digital power-1dBFs
			10.1		dBm	LO=300MHz
			10.4		dBm	LO=700MHz
			9.6		dBm	LO=1800MHz
			9.4		dBm	LO=2600MHz
			6.4		dBm	LO=3600MHz
			6.7		dBm	LO=4600MHz
			4.7		dBm	LO=5500MHz
			4.9		dBm	LO=5800MHz
Third-Order Output intermodulation intercept Point	OIP3					0 dB transmitter attenuation
			28		dBm	LO=300MHz
			27		dBm	LO=700MHz
			26		dBm	LO=1800MHz
			26		dBm	LO=2600MHz
			22		dBm	LO=3600MHz

			22		dBm	LO=4600MHz
			21		dBm	LO=5500MHz
			20		dBm	LO=5800MHz
Carrier Leakage	LOL					With LO leakage correction active, 0 dB attenuation, scales decibel for decibel with attenuation, measured in 1 MHz bandwidth, resolution bandwidth and video bandwidth = 100 kHz, rms detector, 100 trace average
			-78		dBc	LO=300MHz
			-78		dBc	LO=700MHz
			-71		dBc	LO=1800MHz
			-68		dBc	LO=2600MHz
			-65		dBc	LO=3600MHz
			-76		dBc	LO=4600MHz
			-65		dBc	LO=5500MHz
			-65		dBc	LO=5800MHz
Error Vector Magnitude	EVM					3GPP TM3.1A test signal
			1.49		%	LO=2.595GHz
Output impedance	Z_{OUT}		50		Ω	Differential

Table 4

RECEIVERS

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Frequency range		75		6000	MHz	
Gain Range		0		31.5	dB	
Analog Gain Step			0.5		dB	
Bandwidth Ripple			±1		dB	Without bandwidth ripple calibration
Receiver Bandwidth				200	MHz	

Receiver Alias Band Rejection		70			dB	Due to digital filters
Maximum Input Level	P_{HIGH}					0 dB attenuation, CW signal, corresponds to −0.5 dBFS at ADC
			-13.5		dBm	LO=300MHz
			-13.8		dBm	LO=700MHz
			-15.9		dBm	LO=1800MHz
			-14.6		dBm	LO=2600MHz
			-13.1		dBm	LO=3600MHz
			-11.1		dBm	LO=4600MHz
			-9.5		dBm	LO=5500MHz
			-9.9		dBm	LO=5800MHz
Noise Figure	NF					0 dB attenuation, at receiver port
			13.1		dB	LO=700MHz
			12.0		dB	LO=1800MHz
			12.9		dB	LO=2600MHz
			13.3		dB	LO=3600MHz
			15.3		dB	LO=4600MHz
			16.8		dB	LO=5500MHz
			15.7		dB	LO=5800MHz
Third-Order Input Intermodulation Intercept Point	IIP3					Two tone signal, -7dBFs per tone
			12.2		dBm	LO=300MHz
			16.8		dBm	LO=700MHz
			15.4		dBm	LO=1800MHz
			14.8		dBm	LO=2600MHz
			15.8		dBm	LO=3600MHz
			15.8		dBm	LO=4600MHz
			17.1		dBm	LO=5500MHz
			18.2		dBm	LO=5800MHz

Third-Order Harmonic Distortion Product	HD3					-15 dBFs, CW tone at 20MHz offset from LO
			-69.6		dBc	LO=300MHz
			-71.9		dBc	LO=700MHz
			-69.1		dBc	LO=1800MHz
			-70.2		dBc	LO=2600MHz
			-67.3		dBc	LO=3600MHz
			-66.8		dBc	LO=4600MHz
			-68.4		dBc	LO=5500MHz
			-67.0		dBc	LO=5800MHz
Second-Order Intermodulation Distortion	IM2					Two-tone CW signal, -7dBFs with calibration
			63.6		dBc	LO=300MHz
			71.9		dBc	LO=700MHz
			69.9		dBc	LO=1800MHz
			67.4		dBc	LO=2600MHz
			66.9		dBc	LO=3600MHz
			66.5		dBc	LO=4600MHz
			63.5		dBc	LO=5500MHz
			65.0		dBc	LO=5800MHz
Image Rejection						QEC active
			-70.8		dBc	LO=300MHz
			-66.4		dBc	LO=700MHz
			-79.1		dBc	LO=1800MHz
			-75.1		dBc	LO=2600MHz
			-66.5		dBc	LO=3600MHz
			-75.3		dBc	LO=4600MHz
			-69.1		dBc	LO=5500MHz
			-60.1		dBc	LO=5800MHz
Input Impedance			100		Ω	Differential
RX1 to RX2 Isolation			88		dB	LO=300MHz
			84		dB	LO=700MHz

			76		dB	LO=1800MHz
			67		dB	LO=2600MHz
			63		dB	LO=3600MHz
			58		dB	LO=4600MHz
			63		dB	LO=5500MHz
Receiver Band Spurs						-5dBFs receiver signal
			-62		dBc	LO=300MHz
			-65		dBc	LO=700MHz
			-64		dBc	LO=1800MHz
			-60		dBc	LO=2600MHz
			-60		dBc	LO=3600MHz
			-55		dBc	LO=4600MHz
			-54		dBc	LO=5500MHz
			-54		dBc	LO=5800MHz
Receiver DC offset			-66		dBFs	LO=300MHz
			-73		dBFs	LO=700MHz
			-67		dBFs	LO=1800MHz
			-69		dBFs	LO=2600MHz
			-66		dBFs	LO=3600MHz
			-65		dBFs	LO=4600MHz
			-66		dBFs	LO=5500MHz
			-67		dBFs	LO=5800MHz

Table 5

LOCAL OSCILLATOR

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Phase Noise 122.88MHz			-94		dBc/Hz	10Hz offset
			-104		dBc/Hz	100Hz offset
			-114		dBc/Hz	1kHz offset
			-125		dBc/Hz	10kHz offset
			-129		dBc/Hz	100kHz offset
			-143		dBc/Hz	1MHz offset

			-148		dBc/Hz	10MHz offset
Phase Noise 2000MHz			-72		dBc/Hz	10Hz offset
			-81		dBc/Hz	100Hz offset
			-92		dBc/Hz	1kHz offset
			-100		dBc/Hz	10kHz offset
			-104		dBc/Hz	100kHz offset
			-131		dBc/Hz	1MHz offset
			-148		dBc/Hz	10MHz offset
Phase Noise 4000MHz			-66		dBc/Hz	10Hz offset
			-75		dBc/Hz	100Hz offset
			-86		dBc/Hz	1kHz offset
			-94		dBc/Hz	10kHz offset
			-97		dBc/Hz	100kHz offset
			-125		dBc/Hz	1MHz offset
			-144		dBc/Hz	10MHz offset
Phase Noise 6000MHz			-62		dBc/Hz	10Hz offset
			-72		dBc/Hz	100Hz offset
			-82		dBc/Hz	1kHz offset
			-90		dBc/Hz	10kHz offset
			-94		dBc/Hz	100kHz offset
			-118		dBc/Hz	1MHz offset
			-143		dBc/Hz	10MHz offset
LO Phase Synchronization			±5		Degrees	
Lock Time			1.5		ms	
Fast Lock Time			33		us	

Table 6

REFCLK

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Type			LVDS			
Input Frequency		50		1000	MHz	
Signal Level		0.2		0.8	Vpp	

Common-mode Voltage			1.2		V	
Input Differential Impedance			100		Ω	External resistor needed

Table 7

SYSREF_IN

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Type			LVDS			
Signal Level		0.2		0.8	Vpp	
Common-mode Voltage			1.2		V	
Input Differential Impedance			100		Ω	External resistor needed

Table 8

POWER SUPPLY

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
VOLTAGE CHARACTERISTICS						
VDDA1P2 Voltage		1.20	1.25	1.30	V	
VDDD1P0 Voltage		0.90	0.95	1.0	V	
VDDA1P8_Tx Voltage		1.71	1.8	1.89	V	
VDDA1P8_BB Voltage		1.71	1.8	1.89	V	
VDDA_Interface Voltage		1.71	1.8	2.625	V	
VDDA_3P3 Voltage		3.135	3.3	3.456	V	
SUPPLY CURRENT						
VDDA1P2 Current			2.38		A	2TX 450MHz Transmitter Bandwidth, LO=3GHz, input CW=-6dBFs
VDDD1P0 Current			1.91		A	
VDDA1P8 Current			0.41		A	
VDDA_3P3 Current			0.12		A	
Total Power Dissipation			5.8		W	
VDDA1P2 Current			2.18		A	2RX 200MHz Receiver

VDDD1P0 Current			1.36		A	Bandwidth, LO=3GHz, input CW=-6dBFs
VDDA1P8 Current			0.56		A	
VDDA_3P3 Current			0.12		A	
Total Power Dissipation			5.31		W	
VDDA1P2 Current			2.96		A	2TX 450MHz Transmitter Bandwidth, 2RX 200MHz Receiver Bandwidth, LO=3GHz, input CW=-6dBFs
VDDD1P0 Current			2.29		A	
VDDA1P8 Current			0.94		A	
VDDA_3P3 Current			0.12		A	
Total Power Dissipation			7.82		W	

Absolute Maximum Ratings

Table 9

Parameter	Range
VDDA1P2 to VSSA	-0.3V to +1.4V
VDDA1P0 to VSSA	-0.3V to +1.2V
VDDA1P8_Tx , VDDA1P8_BB to VSSA	-0.3V to +2.0V
VDD_Interface to VSSD	-0.3V to +2.8V
VDDA_3P3 to VSSA	-0.3V to +3.9V
Maximum T_J	125℃
Storage Temperature Range	-65℃ to +150℃
Operating Temperature Range	-40~+85℃

Thermal Management

The CBMRF9009 uses an exposed die package to provide the customer with the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly. Figure 5 shows a typical thermal management solution.

To avoid damage, an over-temperature protect mechanism is integrated. When the junction temperature rises over 130 ℃, the transmitters and receivers will be shut down, and the over-temperature status can be read out.

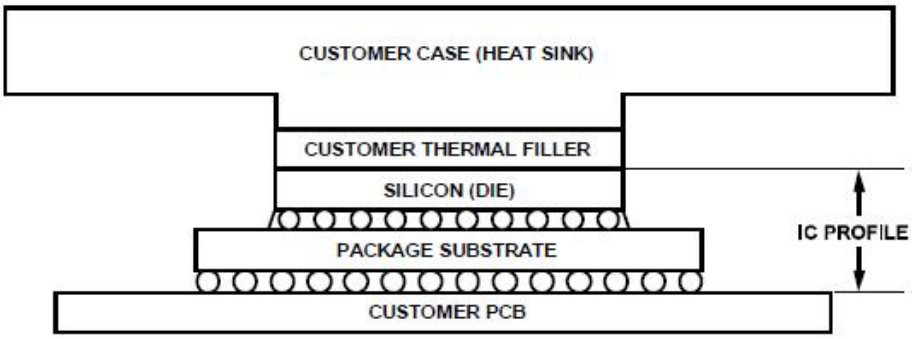

Figure 2 Typical Thermal Management Solution

Thermal Resistance		
Parameter	Type	**Unit**
Rjs	2	K/W
Rjs-top	0.03	K/W

Pin Configuration and Function Descriptions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	ORX2_IN+	ORX2_IN-	VSSA	RX2_IN+	RX2_IN-	VSSA	VSSA	RX1_IN+	RX1_IN-	VSSA	ORX1_IN+	ORX1_IN-	VSSA
B	VDDA1P2_RX_RF	VSSA	VSSA	VSSA	VSSA	VSSA	RF_EXT_LO_I/O-	RF_EXT_LO_I/O+	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
C	GPIO_3P3_0	GPIO_3P3_3	VDDA1P2_RX_TX	VSSA	VDDA1P2_RF_VCO_LDO	VDDA1P2_RF_VCO_LDO	VDDA1P1_RF_VCO	VDDA1P2_RF_LO	VSSA	VDDA1P2_AUX_VCO_LDO	VSSA	VDDA_3P3	GPIO_3P3_9	RBIAS
D	GPIO_3P3_1	GPIO_3P3_4	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VDDA1P1_AUX_VCO_LDO	VSSA	VSSA	GPIO_3P3_8	GPIO_3P3_10
E	GPIO_3P3_2	GPIO_3P3_5	GPIO_3P3_6	VDDA1P8_BB	VDDA1P8_BB	VSSA	REF_CLK_IN+	REF_CLK_IN-	VSSA	AUX_SYNTH_OUT	AUXADC_3	VDDA1P8_TX	GPIO_3P3_7	GPIO_3P3_11
F	VSSA	VSSA	AUXADC_0	AUXADC_1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	AUXADC_2	VSSA	VSSA	VSSA
G	VSSA	VSSA	VSSA	VSSA	VDDA2P2_CLOCK_SYNTH	VSSA	VDDA2P2_RF_SYNTH	VDDA2P2_AUX_SYNTH	RF_SYNTH_VTUNM	VSSA	VSSA	VSSA	VSSA	VSSA
H	TX2_OUT-	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	GPIO_12	GPIO_11	VSSA	TX1_OUT+
J	TX2_OUT+	VSSA	GPIO_18	RESET	GP_INTERRUPT	TEST	GPIO_2	GPIO_1	SDIO	SDO	GPIO_13	GPIO_10	VSSA	TX1_OUT-
K	VSSA	VSSA	SYSREF_IN+	SYSREF_IN-	GPIO_5	GPIO_4	GPIO_3	GPIO_0	SCLK	CS	GPIO_14	GPIO_9	VSSA	VSSA
L	VSSA	VSSA	SYNCIN1-	SYNCIN1+	GPIO_6	GPIO_7	VSSD	VDDD1P0_DIG	VDDD1P0_DIG	VSSD	GPIO_15	GPIO_8	SYNCOUT1-	SYNCOUT1+
M	VDDA1P1_CLOCK_VCO	VSSA	SYNCIN0-	SYNCIN0+	RX1_ENABLE	TX1_ENABLE	RX2_ENABLE	TX2_ENABLE	VSSA	GPIO_17	GPIO_16	VDD_INTERFACE	SYNCOUT0-	SYNCOUT0+
N	VDDA1P2_CLOCK_VCO_LDO	VSSA	SERDOUT3-	SERDOUT3+	SERDOUT2-	SERDOUT2+	VSSA	VDDA1P2_SER	VDDA1P2_DES	SERDIN1-	SERDIN1+	SERDIN0-	SERDIN0+	VSSA
P	AUX_SYNTH_VTUNE	VSSA	VSSA	SERDOUT1-	SERDOUT1+	SERDOUT0-	SERDOUT0+	VDDA1P2_SER	VDDA1P2_DES	VSSA	SERDIN3-	SERDIN3+	SERDIN2-	SERDIN2+

Figure 3 Pin Configuration (Top View)

Table 10 Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Type	Mnemonic	Description
L8, L9	Input	VDDD1P0_DIG	Digital core supply
E5	Input	VDDA1P2_BB	ADC 1.2V supply
N1	Input	VDDA1P2_CLOCK_VCO_LDO	VCO 1.2V supply
B1	Input	VDDA1P2_RX_RF	DAC 1.2V supply
C3	Input	VDDA1P2_RX_TF	Analog 1.2V supply
C10	Input	VDDA1P2_AUX_VCO_LDO	VCO 1.2V supply
C8	Input	VDDA1P2_RF_LO	LO 1.2V supply
C5, C6	Input	VDDA1P2_RF_VCO_LDO	VCO 1.2V supply
N9, P9	Input	VDDA1P2_DES	JESD204B deserializer 1.2V supply
N8, P8	Input	VDDA1P2_SER	JESD204B serializer 1.2V supply
C12	Input	VDDA_3P3	3.3V supply
E12	Input	VDDA1P8_TX	Analog 1.8V supply
E4	Input	VDDA1P8_BB	Digital 1.8V supply
M12	Input	VDD_INTERFACE	Digital IO supply
C7	Output	VDDA1P1_RF_VCO	1.1V output, connect to VSSA through a capacitor
M1	Output	VDDA1P1_CLOCK_VCO	1.1V output, connect to VSSA through a capacitor
D10	Output	VDDA1P1_AUX_VCO	1.1V output, connect to VSSA through a capacitor
G5	Output	VDDA2P2_CLOCK_SYNTH	2.2V output, connect to VSSA through a capacitor
G7	Output	VDDA2P2_RF_SYNTH	2.2V output, connect to VSSA through a capacitor
G8	Output	VDDA2P2_AUX_SYNTH	2.2V output, connect to VSSA through a capacitor
K8	Input/Output	GPIO_0	GPIO
J8	Input/Output	GPIO_1	
J7	Input/Output	GPIO_2	
K7	Input/Output	GPIO_3	

K6	Input/Output	GPIO_4	
K5	Input/Output	GPIO_5	
L5	Input/Output	GPIO_6	
L6	Input/Output	GPIO_7	
L12	Input/Output	GPIO_8	
K12	Input/Output	GPIO_9	
J12	Input/Output	GPIO_10	
H12	Input/Output	GPIO_11	
H11	Input/Output	GPIO_12	
J11	Input/Output	GPIO_13	
K11	Input/Output	GPIO_14	
L11	Input/Output	GPIO_15	
M11	Input/Output	GPIO_16	
M10	Input/Output	GPIO_17	
J3	Input/Output	GPIO_18	
C1	Input/Output	GPIO_3P3_0	GPIO Pin Referenced to 3.3 V Supply
D1	Input/Output	GPIO_3P3_1	
E1	Input/Output	GPIO_3P3_2	
C2	Input/Output	GPIO_3P3_3	
D2	Input/Output	GPIO_3P3_4	
E2	Input/Output	GPIO_3P3_5	
E3	Input/Output	GPIO_3P3_6	
E13	Input/Output	GPIO_3P3_7	
D13	Input/Output	GPIO_3P3_8	
C13	Input/Output	GPIO_3P3_9	
D14	Input/Output	GPIO_3P3_10	
E14	Input/Output	GPIO_3P3_11	
J9	Input/Output	SDIO	Serial Data Input in 4-Wire Mode or Input/Output in 3-Wire Mode
J10	Output	SDO	Serial Data Output. In SPI 3-wire mode, do not connect this pin
K9	Input	SCLK	Serial Data Bus Clock
K10	Input	CS	Serial Data Bus Chip Select, Active Low

M5	Input	RX1_ENABLE	Receiver 1 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground
M6	Input	TX1_ENABLE	Transmitter 1 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground
M7	Input	RX2_ENABLE	Receiver 2 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground
M8	Input	TX2_ENABLE	Transmitter 2 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground
P7	Output	SERDOUT0+	JESD204B output 0 differential pair
P6	Output	SERDOUT0-	
P5	Output	SERDOUT1+	JESD204B output 1 differential pair
P4	Output	SERDOUT1-	
N6	Output	SERDOUT2+	JESD204B output 2 differential pair
N5	Output	SERDOUT2-	
N4	Output	SERDOUT3+	JESD204B output 3 differential pair
N3	Output	SERDOUT3-	
N13	Input	SERDIN0+	JESD204B input 0 differential pair
N12	Input	SERDIN0-	
N11	Input	SERDIN1+	JESD204B input 1 differential pair
N10	Input	SERDIN1-	
P14	Input	SERDIN2+	JESD204B input 2 differential pair
P13	Input	SERDIN2-	
P12	Input	SERDIN3+	JESD204B input 3 differential pair
P11	Input	SERDIN3-	
M14	Output	SYNCOUTB0+	JESD204B sync output 0 differential pair
M13	Output	SYNCOUTB0-	
L14	Output	SYNCOUTB1+	JESD204B sync output 1 differential pair
L13	Output	SYNCOUTB1-	
M4	Input	SYNCINB0+	JESD204B sync input 0 differential pair
M3	Input	SYNCINB0-	
L4	Input	SYNCINB1+	JESD204B sync input 1 differential pair
L3	Input	SYNCINB1-	

J4	Input	RESET	Active low chip reset
J5	Output	GP_INTERRUPT	General-Purpose Digital Interrupt Output Signal
J6	Input	TEST	connect to VSSA through a 1k resistor
C14	Output	RBIAS	Bias Resistor. Tie this pin to ground using a 14.3 kΩ resistor 1%
A9	Input	RX1_IN+	Differential Input for Main Receiver 1
A10	Input	RX1_IN-	
A6	Input	RX2_IN+	Differential Input for Main Receiver 2
A5	Input	RX2_IN-	
A13	Input	ORX1_IN+	Differential Input for Observation Receiver 1
A12	Input	ORX1_IN-	
A2	Input	ORX2_IN+	Differential Input for Observation Receiver 2
A3	Input	ORX2_IN-	
H14	Output	TX1_OUT+	Transmitter 1 Differential Output
J14	Output	TX1_OUT-	
J1	Output	TX2_OUT+	Transmitter 2 Differential Output
H1	Output	TX2_OUT-	
E7	Input	REF_CLK_IN+	Device Clock Differential Input
E8	Input	REF_CLK_IN-	
K3	Input	SYSREF_IN+	SYSREF Differential Input
K4	Input	SYSREF_IN-	
B8	Output	RF_EXT_LO_I/O+	VCO single-ended output
B7	Input	RF_EXT_LO_I/O-	External LO single-ended input, the input frequency must be 2× the desired carrier frequency
P1	Input	AUX_SYNTH_VTUNE	Keep floating
E10	Input	AUX_SYNTH_OUT	Keep floating
G9	Input	RF_SYNTH_VTUNE	Keep floating
F3	Input	AUXADC_0	Auxiliary ADC Input
F4	Input	AUXADC_1	
F11	Input	AUXADC_2	
E11	Input	AUXADC_3	

A1,A4,A7,A8,A11,A14,B2,B3,B4,B5,B6,B9,B10,B11,B12,B13,B14,C4,C9,C11,D3,D4,D5,D6,D7,D8,D9,D11,D12,E6,E9,F1,F2,F5,F6,F7,F8,F9,F10,F12,F13,F14,G1,G2,G3,G4,G6,G10,G11,G12,G13,G14,H2,H3,H4,H5,H6,H7,H8,H9,H10,H13,J2,J13,K1,K2,K13,K14,L1,L2,M2,M9,N2,N7,N14,P2,P3,P10,L7,L10	Input	VSSA	Analog Supply Voltage

Theory of Operation

The CBMRF9009 is a highly integrated, radio frequency (RF), agile transceiver offering dual transmitters, dual receivers, and dual observation receivers, integrated synthesizers, digital signal processing unit and high speed JESD204B interface. The IC can convert analog RF signal to digital baseband IQ data directly.

The digital data interface for the CBMRF9009 uses JEDEC JESD204B Subclass 1. The serial interface consists of four lanes operating at speeds up to 12.288 Gbps. Four high speed serial lanes are provided for the transmitter and four high speed lanes are provided for the observation receiver.

The CBMRF9009 supports very flexible configurations for bandwidth and frequency.The device also supports multichip phase synchronization that synchronizes the phase of the RF local oscillator (LO) and baseband clocks between multiple CBMRF9009 chips.

The flexible and versatile combinations of high performace make CBMRF9009 a comprehensive solution for 3G, 4G, and 5G base station applications.

- **Fequency Synthesizer**

The CBMRF9009 contains three frequency synthesizers, one integer-N frequency synthesizer BBPLL and two fractional-N frequency sythesizers RFPLL. The BBPLL generates all the baseband related clock sources and serialization/deserialization (SERDES) clocks.

The two RFPLLs generate local oscillator (LO) for RF signal paths，and can be configured for transmitters or receivers as LO.

A multichip synchronization mechanism synchronizes the phase of the RF local oscillator (LO) and baseband clocks between multiple CBMRF9009 chips.

- **Transmitter**

The CBMRF9009 transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data from the JESD204B lanes pass through a fully programmable, 128-tap FIR filter with variable interpolation rates. The FIR output is sent to a series of interpolation filters that provide dditional filtering and interpolation prior to reaching the DAC. Each 14-bit DAC has an adjustable sample rate.When converted to baseband analog signals, the inphase (I) and quadrature (Q) signals are filtered to remove sampling artifacts and are fed to the upconversion mixers. Each transmitter chain provides a wide attenuation adjustment range with fine granularity to optimize SNR.

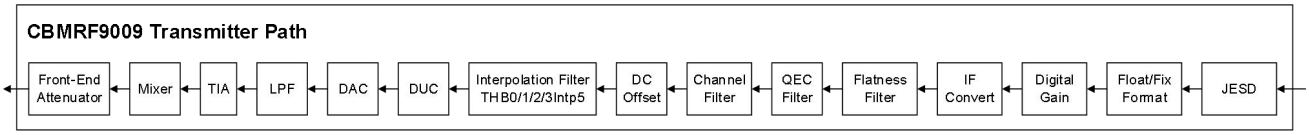

Figure 4 Transmitter path

- **Receiver**

The CBMRF9009 receiver contains all the blocks necessary to receive RF signals and convert them to digital data usable by a BBP. Each receiver can be configured as a direct conversion system that supports up to a 200 MHz bandwidth. Each receiver contains a programmable attenuator stage, followed by matched I and Q mixers that downconvert received signals to baseband for digitization. Gain control can be achieved by using the on-chip AGC or by allowing the BBP to make gain adjustments in a manual gain control mode. Performance is optimized by mapping each gain control setting to specific attenuation levels at each adjustable gain block in the receiver signal path. Additionally, each channel contains independent receive signal strength indicator (RSSI) measurement capability, dc offset tracking, and all circuitry necessary for self calibration.

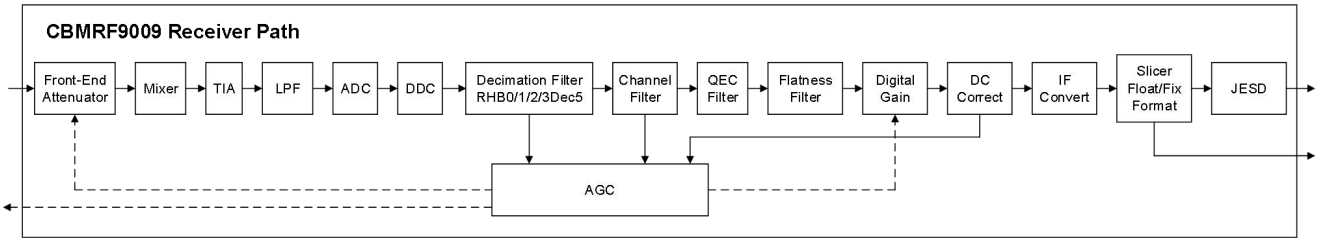

Figure 5 Receiver path

- **Observation Receiver**

The CBMRF9009 observation receiver contains all the blocks necessary to receive RF signals and convert them to digital data usable by a BBP. Each receiver can be configured as a direct conversion system that supports up to a 450 MHz bandwidth. Each receiver contains a programmable attenuator stage, followed by matched I and Q mixers that downconvert received signals to baseband for digitization. Gain control can be achieved by using the on-chip AGC or by allowing the BBP to make gain adjustments in a manual gain control mode. Performance is optimized by mapping each gain control setting to specific attenuation levels at each adjustable gain block in the receiver signal path. Additionally, each channel contains independent receive signal strength indicator (RSSI) measurement capability, dc offset tracking, and all circuitry necessary for self calibration.

Outline Dimensions

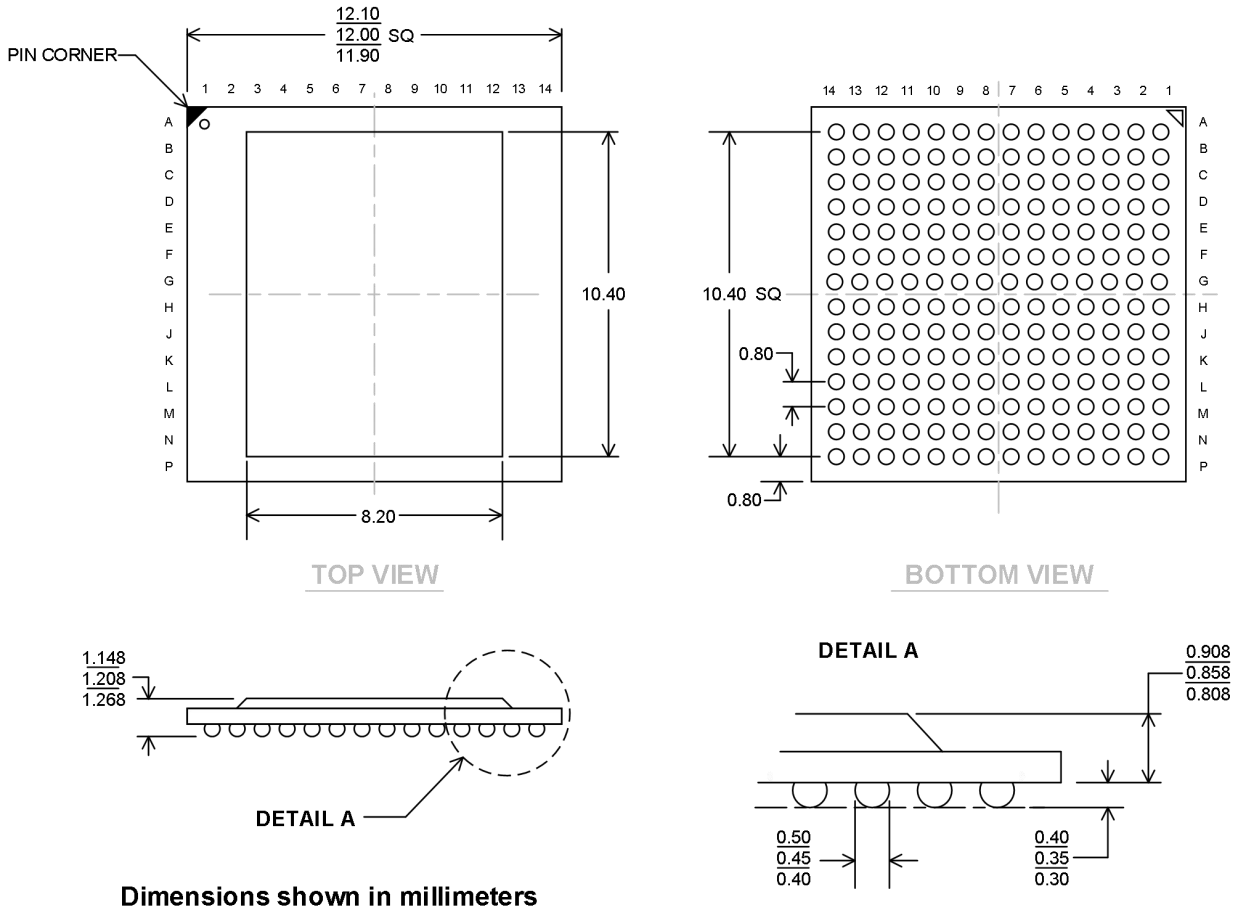

Figure 6 196-Ball Flip Chip Ball Grid Array [CSP_BGA]

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION	MAKING INFORMATION
CBMRF9009BG		-40℃~85℃	CSP_BGA 196		