Features

- Analog Power Supply Voltages: 3.3V, 1.8V, 1.3V
- Digital Power Supply Voltage: 1.3V
- RF 2×2 Transceiver with Integrated 12-bit DAC and ADC
- Frequency Band: 70 MHz to 6.0 GHz
- Supports TDD and FDD
- Tunable Channel Bandwidth: <200 kHz to 56 MHz
- TX EVM: −40 dB
- Circuit Interface: CMOS/LVDS Digital Interface
- ESD Rating: HBM 500V

Applications

- Point-to-point communication system
- Microcell base station
- Universal radio system

General Description

CBMRF001 is a high-performance, highly integrated radio frequency (RF) agile transceiver for 3G and 4G base station applications. The programmability and wideband capability of this device make it an ideal choice for a variety of transceiver applications. The device integrates the RF front-end with a flexible mixed-signal baseband section, incorporates a frequency synthesizer, and provides a configurable digital interface for the processor, thereby simplifying design implementation. The CBMRF001 operates in the frequency range from 70 MHz to 6.0 GHz, covering most licensed and unlicensed frequency bands, and supports a channel bandwidth range from less than 200 kHz to 56 MHz. The two independent direct-conversion receivers feature leading noise figure and linearity. Each receive (RX) subsystem has independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital filtering functions, eliminating the need to provide these functions in the digital baseband. The CBMRF001 also has a flexible manual gain mode that supports external control. Each channel is equipped with two high dynamic range ADCs, which first digitize the received I and Q signals, then pass them through a configurable decimation filter and a 128-tap finite impulse response (FIR) filter, and generate 12-bit output signals at the corresponding sampling rate.

The transmitter adopts a direct-conversion architecture, which can achieve high modulation accuracy and ultra-low noise. This transmitter design results in a TX EVM of less than <−40 dB,

leaving considerable system margin for the selection of external power amplifiers. The on-board transmit (TX) power monitor can be used as a power detector to achieve highly accurate TX power measurement.

A fully integrated phase-locked loop (PLL) provides low-power fractional-N frequency synthesis for all receive and transmit channels. The design integrates the channel isolation required by frequency division duplex (FDD) systems. All VCO and loop filter devices are also integrated. The circuit uses a 10mm×10mm, 144-pin chip-scale ball grid array package (CSP_BGA). This product can effectively replace AD9361 from ADI.

Catalog

Functional Block Diagram

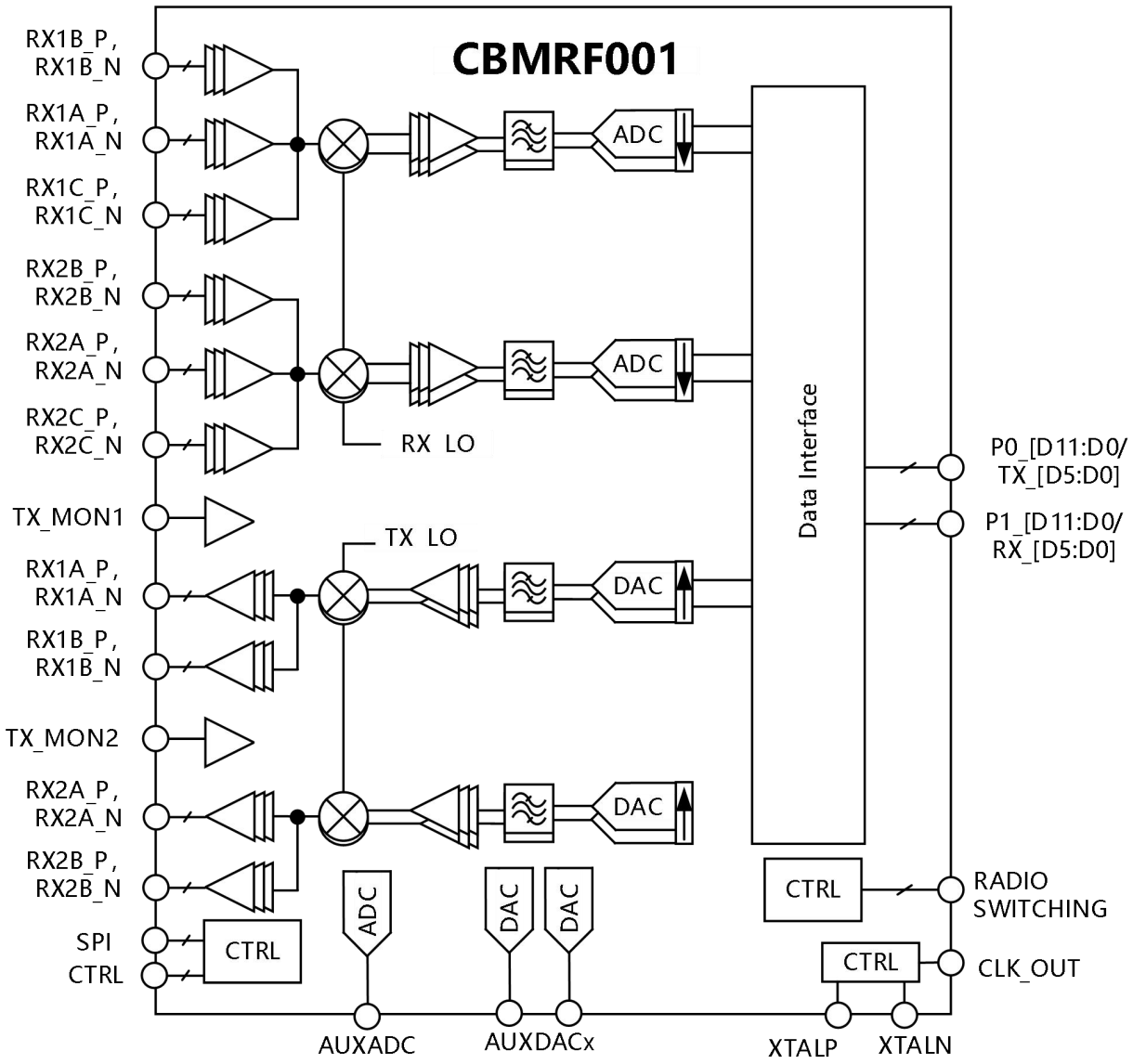


Figure 1. Functional Block Diagram

Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Receiver, generally					
Center Frequency		70	--	6000	MHz
Gain	800MHz	0	--	71.5	dB
	2300 MHz (RX1A, RX2A)	--	70	--	dB
	2300 MHz (RX1B,RX1C, RX2B, RX2C)	--	70	--	dB
	5500 MHz (RX1A, RX2A)	--	62	--	dB
Gain Step		--	1	--	dB
RSSI Level		--	95	--	dB
RSSI Accuracy		--	±2.5	--	dB
Receiver, 800MHz					
Noise Figure (NF)	Maximum RX Gain	--	2.8	--	dB
Third-Order Input Intercept Point (IIP3)	Maximum RX Gain	--	-11	--	dBm
Second-Order Input Intercept Point (IIP2)	Maximum RX Gain	--	55	--	dBm
Local Oscillator (LO) Leakage	RX front-end input	--	-82	--	dBm
Quadrature Gain Error		--	0.2	--	%
Quadrature Phase Error		--	0.2	--	度
Modulation Accuracy (EVM, Error Vector Magnitude)	40 MHz reference clock	--	(not tested yet)	--	dB
Input S11		--	(not tested yet)	--	dB
RX1 to RX2 Isolation (RX1A to RX2A, RX1C to RX2C)		--	55	--	dB
RX1 to RX2 Isolation (RX1B to RX2B)		--	50	--	dB
RX2 to RX1 Isolation (RX2A to		--	55	--	dB

RX1A, RX2C to RX1C)					
RX2 to RX1 Isolation (RX2B to RX1B)		--	50	--	dB
Receiver，5.5 GHz					
Noise Figure (NF)	Maximum RX Gain	--	4	--	dB
Third-Order Input Intercept Point (IIP3)	Maximum RX Gain	--	-4	--	dBm
Second-Order Input Intercept Point (IIP2)	Maximum RX Gain	--	58	--	dBm
Local Oscillator (LO) Leakage	RX front-end input	--	-75	--	dBm
Quadrature Gain Error		--	0.2	--	%
Quadrature Phase Error		--	0.2	--	度
Modulation Accuracy (EVM, Error Vector Magnitude)	40 MHz reference clock	--	(not tested yet)	--	dB
Input S11		--	(not tested yet)	--	dB
RX1A to RX2A Isolation		--	50	--	dB
RX2A to RX1A Isolation		--	37	--	dB
Receiver，generally					
Center Frequency		70	--	6000	MHz
Power Control Range		--	90	--	dB
Power Control Resolution		--	0.25	--	dB
Transmitter，800 MHz					
Output S22		--	not tested yet	--	dB
Maximum Output Power	1 MHz tone (50Ω load)	--	8	--	dBm
Modulation Accuracy (EVM, Error Vector Magnitude)	19.2 MHz reference clock	--	-45	--	dB
Third-Order Output Intercept Point (OIP3)		--	17	--	dBm

Carrier Leakage	0 dB attenuation	--	-50	--	dBc
	40 dB attenuation	--	-40	--	dBc
Noise Floor	90 MHz offset	--	-148	--	dBm/Hz
Isolation (TX1 to TX2)		--	50	--	dB
Isolation (TX2 to TX1)		--	50	--	dB
Transmitter，2.4GHz					
Output S22		--	not tested yet	--	dB
Maximum Output Power	1 MHz tone (50Ω load)	--	7	--	dBm
Modulation Accuracy (EVM, Error Vector Magnitude)	40 MHz reference clock	--	-40	--	dB
Third-Order Output Intercept Point (OIP3)		--	17.5	--	dBm
Carrier Leakage	0 dB attenuation	--	-50	--	dBc
	40 dB attenuation	--	-44	--	dBc
Noise Floor	90 MHz offset	--	-138	--	dBm/Hz
Isolation (TX1 to TX2)		--	50	--	dB
Isolation (TX2 to TX1)		--	50	--	dB
Transmitter，5.5GHz					
Output S22		--	not tested yet	--	dB
Maximum Output Power	77 MHz tone (50Ω load)	--	7	--	dBm
Modulation Accuracy (EVM, Error Vector Magnitude)	40 MHz reference clock（For internal doubling in RF frequency synthesizer)	--	-40	--	dB
Third-Order Output Intercept Point (OIP3)		--	17.5	--	dBm
Carrier Leakage	0 dB attenuation	--	-50	--	dBc
	40 dB attenuation	--	-44	--	dBc
Noise Floor	90 MHz offset	--	-138	--	dBm/Hz
Isolation (TX1 to TX2)		--	50	--	dB

Isolation (TX2 to TX1)		--	50	--	dB

Recommended Operating Conditions

- VDD_GPO = 3.3V
- VDD_INTERFACE = 1.8V
- All other VDDx pins = 1.3V
- Temperature: 25°C
- Input reference clock: 40MHz

Absolute Maximum Ratings

- VDDx to VSSx: −0.3 V to +1.4 V
- VDD_INTERFACE to VSSx: −0.3 V to +3.0 V
- VDD_GPO to VSSx: −0.3 V to +3.9 V
- Logic inputs and outputs to VSSx: −0.3 V to VDD_INTERFACE + 0.3 V
- Input current to any pin except power pins: ±10 mA
- RF input (peak power): 2.5 dBm
- TX monitor input power (peak power): 9 dBm
- Package power dissipation: (TJMAX − TA)/θJA
- Junction temperature (TJ): 110°C
- Operating temperature range: -40°C ~ 85°C
- Storage temperature (Tstg): -65°C ~ 150°C

Pin Configurations and Function Descriptions

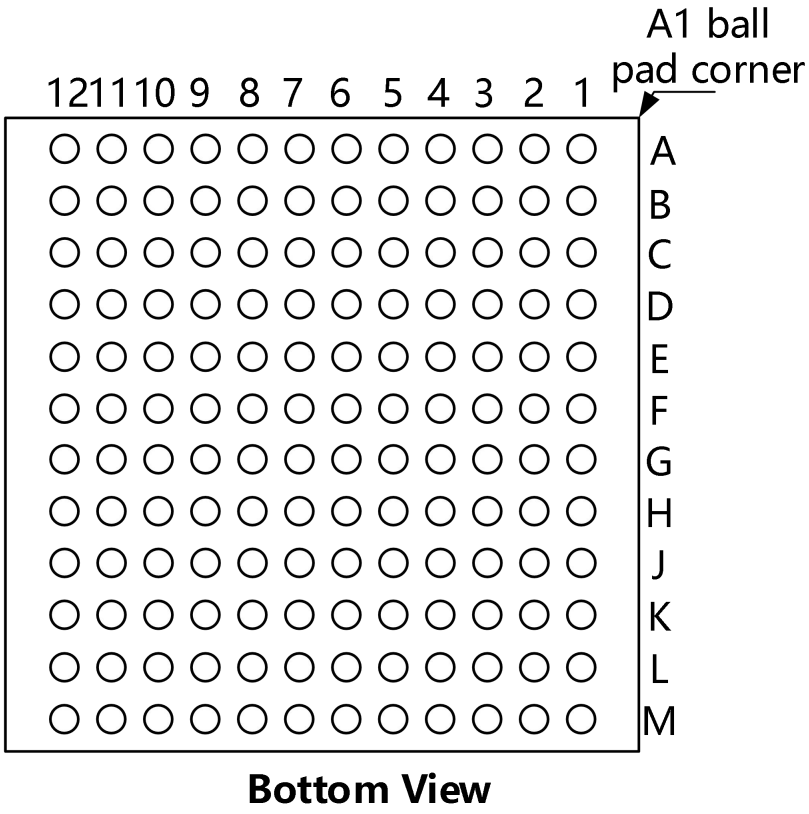


Figure 2. Pin assignment

Pin Number	Pin Type	Pin Name	Description
A1, A2	I	RX2A_N, RX2A_P	Receiver Channel 2 Differential Input A. Alternatively, each pin can be used as a single-ended input or combined to form a differential pair. Ground the unused pins.
A3, M3	NC	NC	No connection. Do not connect to these pins.
A4, A6, B1,B2, B12, C2, C7 to C12, F3, H2, H3, H6, J2, K2, L2, L3, L7 to L12, M4,M6	I	VSSA	Analog ground. Connect these pins directly to the VSSD digital ground (a ground plane) on the printed circuit board.
A5	I	TX_MON2	Transmit Channel 2 Power Monitor Input. If this pin is not used, ground it.

A7, A8	O	TX2A_N, TX2A_P	Transmit Channel 2 Differential Output A. Connect unused pins to 1.3V.
A9, A10	O	TX2B_N, TX2B_P	Transmit Channel 2 Differential Output B. Connect unused pins to 1.3V.
A11	I	VDDA1P1_TX_VCO	Transmit VCO power input. Connect to B11.
A12	I	TX_EXT_LO_IN	External transmit LO input. If this pin is not used, ground it.
B3	O	AUXDAC1	Auxiliary DAC 1 Output.
B4 to B7	O	GPO_3 to GPO_0	General-purpose outputs supporting 3.3 V.
B8	I	VDD_GPO	2.5 V to 3.3 V power supply, supporting AUXDAC and general-purpose output pins. When the VDD_GPO power supply is not in use, this power supply must be set to 1.3 V.
B9	I	VDDA1P3_TX_LO	Transmit LO 1.3V power - input.
B10	I	VDDA1P3_TX_VCO _LDO	Transmit VCO LDO 1.3 V power input. Connect to B9.
B11	O	TX_VCO_LDO_OUT	Transmit VCO LDO output. Connect to A11, and connect a 1 μF bypass capacitor in series with a 1 Ω resistor to ground.
C1,D1	I	RX2C_P, RX2C_N	Receiver Channel 2 Differential Input C. Each pin can be used as a single - ended input or combined to form a differential pair. The performance of these inputs will degrade above 3 GHz. Ground the unused pins.
C3	O	AUXDAC2	Auxiliary DAC 2 Output.
C4	I	Test/Enable	Test input. During normal operation, ground this pin.
C5, C6, D5, D6	I	CTRL_IN0 to CTRL_IN3	Control inputs. Used for manual RX gain and TX attenuation control.
D2	I	VDDA1P3_RX_RF	Receiver 1.3 V power input. Connect to D3.
D3	I	VDDA1P3_RX_TX	1.3 V power input.
D4，E4 to F4 to F6，G4	O	CTRL_OUT0，CTRL_OUT1 to CTRL_OUT3，CTRL_OUT6 to CTRL_OUT4，CTRL_OUT7	Control outputs. These pins are multi-functional outputs with programmable features.
D7	I/O	P0_D9/TX_D4_P	Digital Data Port P0/Transmit Differential Input Bus. This is a

			dual-function pin. For P0_D9, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D4_P) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
D8	I/O	P0_D7/TX_D3_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D7, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D3_P) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
D8	I/O	P0_D5/TX_D2_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D5, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D2_P) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
D10	I/O	P0_D3/TX_D1_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D3, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D1_P) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
D11	I/O	P0_D1/TX_D0_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D1, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D0_P) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
D12, F7, F9,F11, G12, H7, H10, K12	I	VSSD	Digital ground. Connect these pins directly to the VSSA analog ground (a ground plane) on the printed circuit board.
E1, F1	I	RX2B_P, RX2B_N	Receive Channel 2 Differential Input B. Each pin can be used as a single-ended input or combined to form a differential pair. The performance of these inputs will degrade above 3 GHz. Ground any unused pins.
E2	I	VDDA1P3_RX_LO	Receive LO 1.3 V power input.
E3	I	VDDA1P3_TX_LO_BUFFER	1.3 V power input.

E7	I/O	P0_D11/TX_D5_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D11, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D5_P) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E8	I/O	P0_D8/TX_D4_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D8, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D4_N) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E9	I/O	P0_D6/TX_D3_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D6, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D3_N) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E10	I/O	P0_D4/TX_D2_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D4, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D2_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E11	I/O	P0_D2/TX_D1_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D2, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D1_N) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E12	I/O	P0_D0/TX_D0_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D0, it acts as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D0_N) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
F2	I	VDDA1P3_RX_VCO_LDO	Receive VCO LDO 1.3 V power input. Connect to E2.
F8	I/O	P0_D10/TX_D5_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual-function pin. For P0_D10, it acts as part of the 12-bit

			bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D5_N) can also serve as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
F10, G10	I	FB_CLK_P,FB_CLK_N	Feedback Clock. These pins receive the FB_CLK signal, which serves as the TX data clock. In CMOS mode, use FB_CLK_P as the input and ground FB_CLK_N.
F12	I	VDDD1P3_DIG	1.3 V digital power input.
G1	I	RX_EXT_LO_IN	External receive LO input. If this pin is not used, ground it.
G2	O	RX_VCO_LDO_OUT	Receive the output of the VCO LDO. Connect this pin directly to G3, and connect a 1 μF bypass capacitor in series with a 1Ω resistor to ground.
G3	I	VDDA1P1_RX_VCO	Receive the power - input for VCO. Connect this pin directly only to G2.
G5	I	EN_AGC	Manual control input for Automatic Gain Control (AGC).
G6	I	使能	Control Input. This pin enables the device to shift between various operating states.
G7, G8	O	RX_FRAME_N, RX_FRAME_P	Receive Digital Data Frame Output Signal. These pins emit the RX_FRAME signal, which is used to indicate whether the RX output data is valid. In CMOS mode, use RX_FRAME_P as the output and keep RX_FRAME_N open.
G9, H9	I	TX_FRAME_P, TX_FRAME_N	Transmit Digital Data Frame Input Signal. These pins receive the TX_FRAME signal used to indicate when TX data is valid. In CMOS mode, use TX_FRAME_P as the input and ground TX_FRAME_N.
G11, H11	O	DATA_CLK_P, DATA_CLK_N	Receive Data Clock Output. These pins emit the DATA_CLK signal, and the BBP uses these signals to clock the RX data. In CMOS mode, use DATA_CLK_P as the output and keep DATA_CLK_N open.
H1,J1	I	RX1B_P, RX1B_N	Receive Channel 1 Differential Input B. Additionally, each pin can be used as a single-ended input. The performance of these inputs will degrade above 3 GHz. Ground unused pins.
H4	I	TXNRX	Enable state machine control signal. This pin controls the direction of the data port bus. A logic low level selects the RX direction, and a logic high level selects the TX direction.

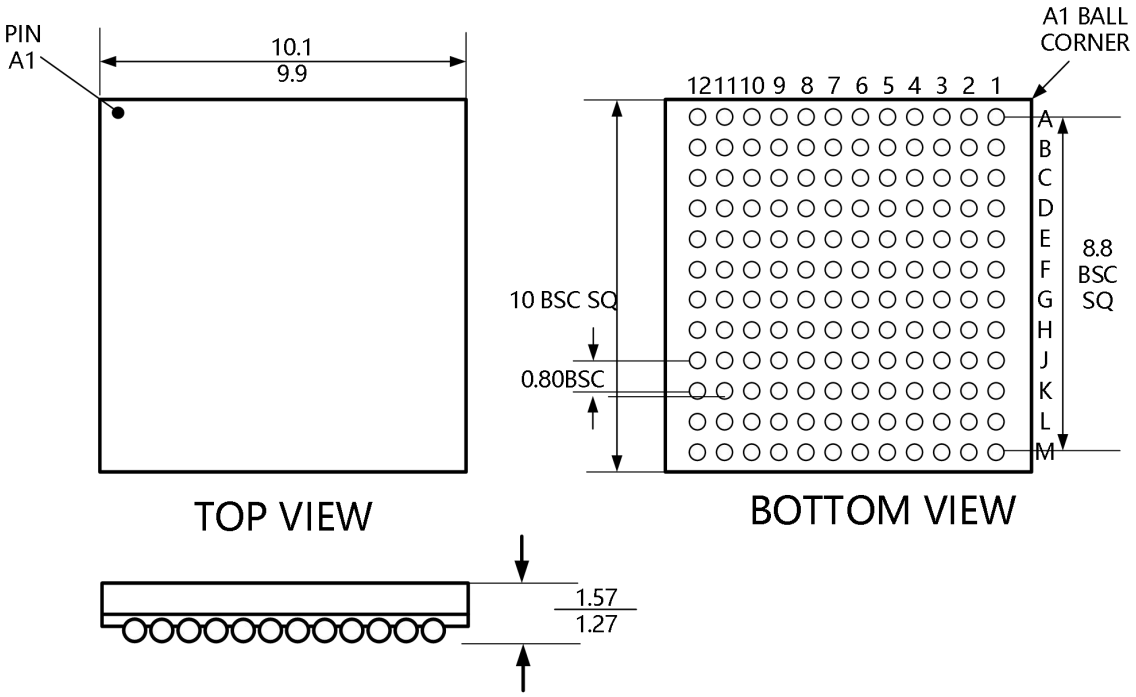
H5	I	SYNC_IN	Input for synchronizing digital clocks among multiple CBMRF001 devices. If this pin is not used, it should be grounded.
H8	I/O	P1_D11/RX_D5_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual-function pin. For P1_D11, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D5_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
H12	I	VDD_INTERFACE	Digital I/O pin, 1.2 V to 2.5 V power supply (1.8 V to 2.5 V in LVDS mode).
J3	I	VDDA1P3_RX_SYNTH	1.3 V power supply input.
J4	I	SPI_DI	SPI serial data input
J5	I	SPI_CLK	SPI clock input.
J6	O	CLK_OUT	Output clock. This pin can be configured to output a buffered version of the external input clock DCXO, or an output divided version of the internal ADC_CLK.
J7	I/O	P1_D10/RX_D5_N	Digital Data Port P1/Receive Differential Output Bus. This is a dual-function pin. For P1_D10, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D5_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J8	I/O	P1_D9/RX_D4_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual-function pin. For P1_D9, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D4_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J9	I/O	P1_D7/RX_D3_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual-function pin. For P1_D7, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D3_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J10	I/O	P1_D5/RX_D2_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual-function pin. For P1_D5, it serves as part of the 12-bit

			bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D2_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J11	I/O	P1_D3/RX_D1_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual-function pin. For P1_D3, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D1_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J12	I/O	P1_D1/RX_D0_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual-function pin. For P1_D1, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D0_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K1, L1	I	RX1C_P, RX1C_N	Receive Channel 1 Differential Input C. Additionally, each pin can be used as a single-ended input. The performance of these inputs will degrade above 3 GHz. Ground unused pins.
K3	I	VDDA1P3_TX_SYNTH	1.3 V power supply input.
K4	I	VDDA1P3_BB	1.3 V power supply input.
K5	I	RESETB	Asynchronous reset. A logic low level resets the device.
K6	I	SPI_ENB	SPI Enable Input. Drive this pin low to enable the SPI bus.
K7	I/O	P1_D8/RX_D4_N	Digital Data Port P1/Receive Differential Output Bus. These are dual-function pins. For P1_D8, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D4_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K8	I/O	P1_D6/RX_D3_N	Digital Data Port P1/Receive Differential Output Bus. These are dual-function pins. For P1_D6, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D3_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K9	I/O	P1_D4/RX_D2_N	Digital data port P1/receive differential output bus. This is a dual-function pin. For P1_D4, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this

			pin (RX_D2_N) can also serve as part of the LVDS 6-bit RX differential output bus (with internal LVDS terminals).
K10	I/O	P1_D2/RX_D1_N	Digital Data Port P1/Receive Differential Output Bus. These are dual-function pins. For P1_D2, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D1_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K11	I/O	P1_D0/RX_D0_N	Digital Data Port P1/Receive Differential Output Bus. These are dual-function pins. For P1_D0, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D0_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
L4	I	RBIAS	Bias input reference. Ground this pin through a 14.3 kΩ (1% tolerance) resistor.
L5	I	AUXADC	Auxiliary ADC Input. Ground this pin if unused.
L6	O	SPI_DO	SPI serial data output in 4-wire mode, or high-Z in 3-wire mode.
M1, M2	I	RX1A_P, RX1A_N	Receive Channel 1 Differential Input A. In addition, each pin can be used as a single-ended input. Ground unused pins.
M5	I	TX_MON1	Transmit Channel 1 Power Monitor Input. Ground this pin when unused.
M7, M8	O	TX1A_P, TX1A_N	Transmit Channel 1 Differential Output A. Connect unused pins to 1.3 V.
M9, M10	O	TX1B_P, TX1B_N	Transmit Channel 1 Differential Output B. Connect unused pins to 1.3 V.
M11, M12	I	XTALP, XTALN	Reference frequency crystal oscillator connection. When using a crystal oscillator, connect it between these two pins. When using an external clock source, connect it to XTALN and leave XTALP disconnected.
This translation maintains the standard electrical engineering abbreviations while providing their full English equivalents.			

Outline Dimensions

BGA-144



Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION	MAKING INFORMATION
CBMRF001		-40℃~85℃	BGA-144		

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.7.2		Regular update	WW	LYL	Initial Version