Features

- **Two low-noise programmable gain amplifiers (PGA) and two high resolution synchronous sampling analog-to-digital converters (ADC)**
- **Input-referred noise: 1.2 uVpp (at 70 Hz bandwidth)**
- **Input bias current: 300 pA**
- **Data rate: 250 ~ 16000 samples per second (SPS)**
- **Common-mode rejection ratio (CMRR): -120 dB**
- **Programmable gain: 1, 2, 4, 6, 8, 12, or 24**
- **Unipolar or bipolar supply:**
  - ✧ **Analog: 4.75 V to 5.25 V**
  - ✧ **Digital: 1.8 V to 3.6 V**
- **Integrated functions for human bio-signal measurement:**
  - ✧ **Human bias amplifier**
  - ✧ **Lead-off detection**
  - ✧ **Internal test signal**
- **Optional internal oscillator**
- **Optional internal reference**
- **Flexible power-down and standby modes**
- **SPI interface**
- **Operating temperature range: -40°C ~ +85°C**

Application

- Medical devices for human bioelectric signal measurement:
- Electroencephalogram (EEG) research
- Fetal electrocardiogram (ECG) monitoring
- Sleep study monitoring
- Bispectral Index (BIS)
- Evoked Audio Potentials (EAP)

Description

CBM24AD92-2CQ is a 2-channel, low-noise, 24-bit synchronous sampling delta-sigma analog-to-digital converter (ADC). The device integrates a programmable gain amplifier (PGA), internal reference, and clock oscillator. CBM24AD92-2CQ provides the features required for extracranial EEG and ECG applications. With high integration and superior performance, CBM24AD92-2CQ enables users to build wearable brain-computer interface systems in a much smaller form factor.

CBM24AD92-2CQ is equipped with a flexible input multiplexer for each channel. The multiplexer can be independently connected to internally generated signals to perform test, temperature, and lead-off detection.

In addition, the body bias output signal can be generated from any configuration of the input channels. Optional SRB1/2 pins are also available to serve as the opposite input for single-ended (P/N) sampling. Channel 1 can

be configured for respiration detection mode if required.

The CBM24AD92-2CQ operates at a data transfer rate ranging from 250 SPS to 16 kSPS. Lead-off detection can be implemented internally in the device via an excitation current source. Multiple CBM24AD92-2CQ devices can be connected in series using a daisy-chain configuration in systems with a large number of channels. The CBM24AD92-2CQ is available in VQFN-32 (5mm*5mm) and TQFP-32 packages.

Datalog

Revision History

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2026.3.2			WW	LYL	

Functional Block Diagram

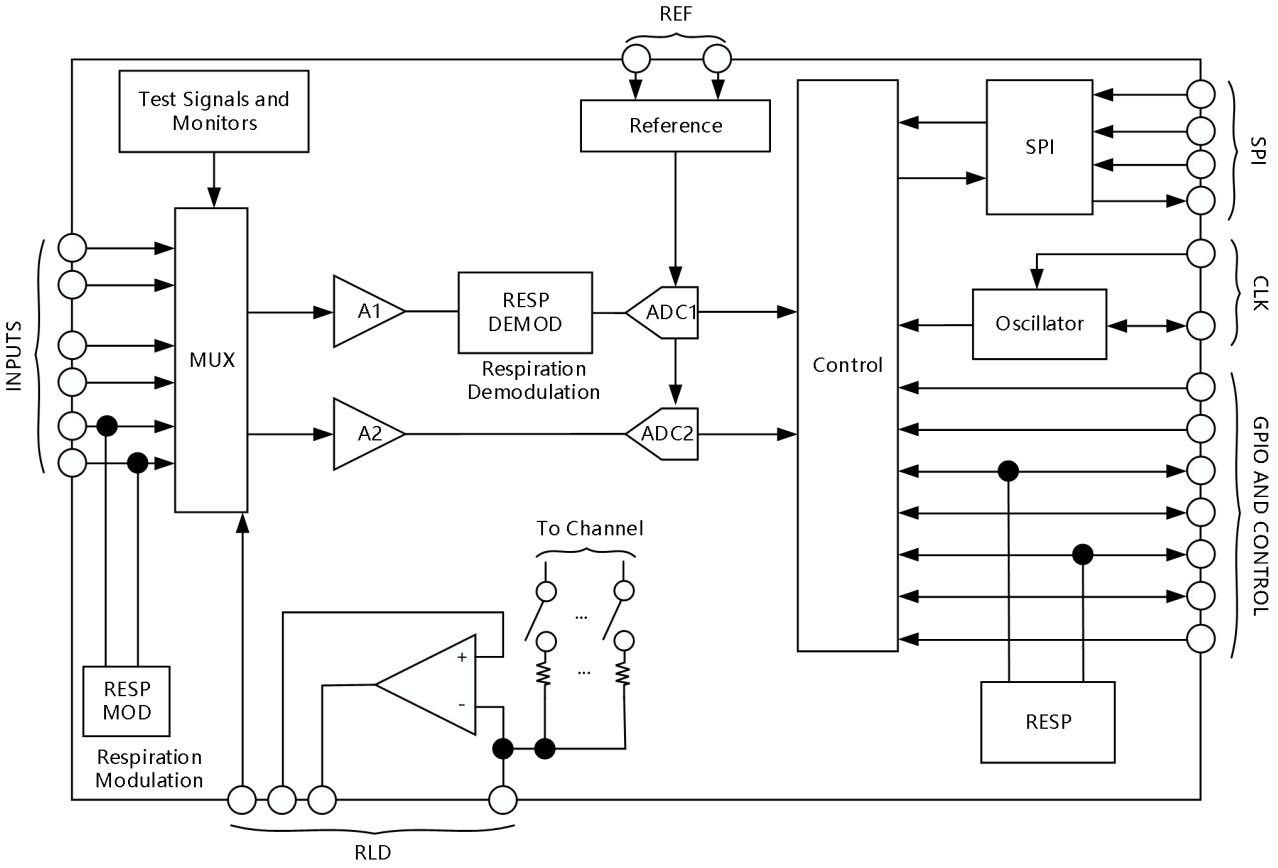


Figure 1. Functional Block Diagram

Pin Configuration and Function Descriptions

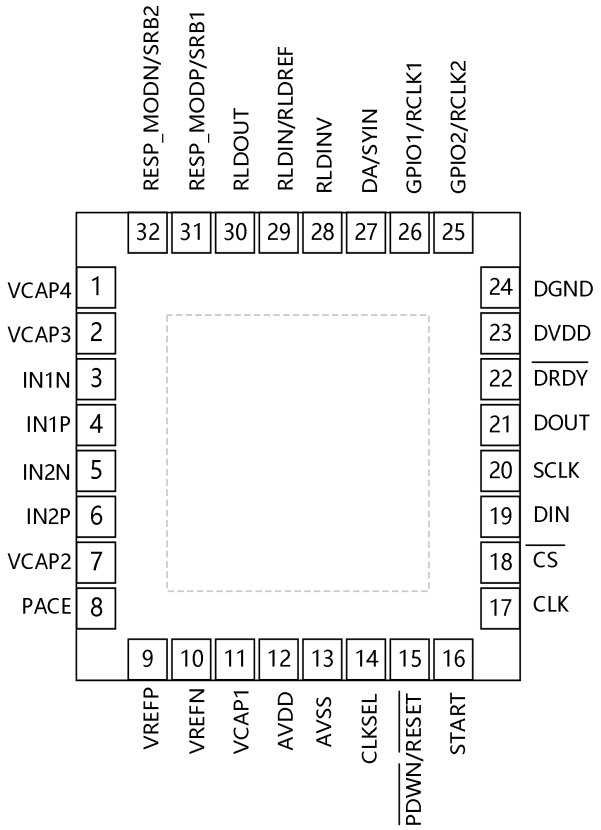


Figure 2. VQFN-32 Pin Configuration (Top View)

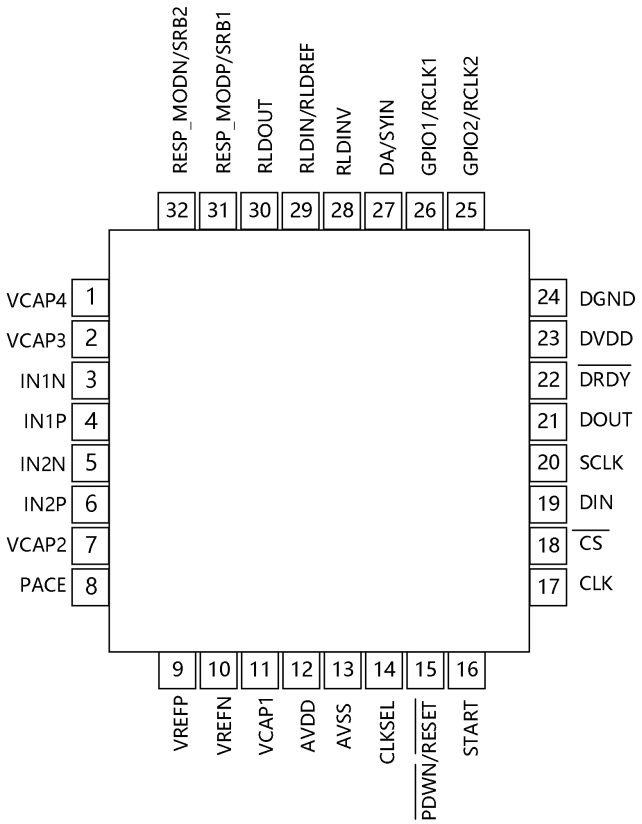


Figure 3. TQFP-32 Pin Configuration (Top View)

Pin No.	Type	Pin Name (VQFN-32/TQFP-32)	Description
1	Analog Output	VCAP4	Analog capacitor pin; connect a 1 μF capacitor to AVSS.
2	Analog Output	VCAP3	Analog capacitor pin; connect a parallel combination of 1 μF and 0.1 μF capacitors to AVSS.
3	Analog Input	IN1N	Channel 1 differential analog negative input
4	Analog Input	IN1P	Channel 1 differential analog positive input
5	Analog Input	IN2N	Channel 2 differential analog negative input
6	Analog Input	IN2P	Channel 2 differential analog positive input
7	Analog	VCAP2	Analog capacitor pin; connect a 1 μF capacitor to AVSS.

	Output		
8	Analog Output	PACE	Pacemaker detection analog output
9	Analog Input/Output	VREFP	Positive analog reference voltage; connect a capacitor of at least 10 μF to VREFN.
10	Analog Input	VREFN	Negative analog reference voltage.
11	Analog Output	VCAP1	Analog capacitor pin; connect a 10 μF capacitor to AVSS.
12	Analog Power	AVDD	Analog Power; connect a 1 μF capacitor to AVSS.
13	Analog GND	AVSS	Analog GND
14	Digital Input	CLKSEL	Internal or external main clock selection
15	Digital Input	$\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ or RESET_/PWDN_	System reset, active low
16	Digital Input	START	Synchronization signal to start or restart conversion
17	Digital Input	CLK	Main clock input
18	Digital Input	$\overline{\text{CS}}$ or CS_	SPI chip select, active low
19	Digital Input	DIN	SPI serial data input
20	Digital Input	SCLK	SPI serial clock input
21	Digital Output	DOUT	SPI serial data output
22	Digital Output	$\overline{\text{DRDY}}$或DRDY_	Data ready, active low
23	Digital Power	DVDD	Digital Power; connect a 1 μF capacitor to DGND.
24	Digital GND	DGND	Digital GND
25	Digital Input/Output	GPIO2	General-purpose input/output pin 2
26	Digital Input/Output	GPIO1	General-purpose input/output pin 1
27	Digital Input	DAISYIN	Daisy-chain input
28	Analog Input/Output	BIASINV or RLDINV	Inverting input of body bias or right leg drive op-amp

29	Analog Input	BIASIN/BIASREF or RLDIN/RLDRE	Reference input of body bias or right leg drive op-amp
30	Analog Output	BIASOUT or RLDOUT	Output of body bias or right leg drive op-amp
31	Analog Input/Output	RESP_MODEP/SRB1	Reference and bias signal 1 or respiration modulation signal P
32	Analog Input/Output	RESP_MODEN/SRB2	Reference and bias signal 2 or respiration modulation signal N

Absolute maximum rating

Parameter	Range
AVDD to AVSS	-0.3V to +5.5V
DVDD to DGND	-0.3V to +3.9V
AVSS to DGND	-3V to +0.2V
VREFP to AVSS	-0.3V to AVDD+0.3V
VREFN to AVSS	-0.3V to AVDD+0.3V
Analog Input	AVSS-0.3 to AVDD+0.3V
Digital Input	DGND-0.3 to DVDD+0.3V
Input, continuous, any pin except power supply pins	-10 to 10mA
Junction Temperature , T_J	150℃
Storage Temperature , Tstg	-65℃ to +150℃
HBM	±2kV
CDM	±500V

Recommended operating conditions

Parameter		Min	Typ	Max	Unit
Supply Range					
Analog Supply	AVDD to AVSS	4.75	5	5.25	V
Digital Supply	DVDD to DGND	1.8	3.3	3.6	V
Analog-to-Digital Supply Voltage Difference	AVDD – DVDD	-2.1	--	3.6	V
Analog Input Range					

Full-scale differential input voltage	VINxP - VINxN	--	±VREF / Gain	--	V
Input signal common-mode voltage range (VCM)	(VINxP + VINxN) / 2				V
Reference Voltage Input Range					
Reference Input Voltage (VREF)	VREF = (VVREFP - VVREFN)	--	4.5	--	V
Negative Input (VREFN)		--	AVSS	--	V
Positive Input (VREFP)		--	AVSS+4.5	--	V
Clock Input					
External Clock Input Frequency	CLKSEL pin = 0	1.5	2.048	2.25	MHz
Digital Input					
Input Voltage Range		DGND - 0.1	--	DVDD + 0.1	V
Temperature Range					
Operating Temperature Range (T_A)		-40	--	85	℃

Thermal Performance Parameters

Thermal Performance Parameters		Unit
$R_{\theta JA}$ Junction-to-ambient thermal resistance	46.2	°C/W
$R_{\theta JC(top)}$ Junction-to-case(top) thermal resistance	5.8	
$R_{\theta JC(bot)}$ Junction-to-case(bottom) thermal resistance	--	
$R_{\theta JB}$ Junction-to-board thermal resistance	19.6	
ψ_{JT} Junction-to- top characterization parameter	0.2	
ψ_{JB} Junction-to- board characterization parameter	19.2	

Electrical Characteristics

Unless otherwise noted, typical values are specified at T_A=25°C. The minimum and maximum values apply over the temperature range of T_A=-40°C to +85°C.All electrical parameters are measured under the following conditions:AVDD-AVSS=5V, DVDD=3.3V, VREF=4.6V, external clock with f_{CLK}=2.048MHz, data rate=250SPS, gain=12.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Analog Input						
Input Capacitance		--	20	--	pF	
Input Bias Current		--	--	±300	pA	T_A = 25°C, INxP = INxN = 2.5V
		--	±300	--	pA	T_A = -40°C ~ +85°C, INxP = INxN = 2.5V
DC Input Resistance		--	1000	--	MΩ	Not enabled lead-off
		--	--	500		$I_{LEADOFF}$ = 6nA
PGA performance						
Gain settings		1, 2, 4, 6, 8, 12, 24				
Bandwidth	BW	662 / 332 / 165 / 110 / 83 / 55 / 27 @Gain = 1 / 2 / 4 / 6 / 8 / 12 / 24			kHz	
ADC performance						
Resolution		--	24	--	Bits	
Sampling Rate	DR	250	--	16000	SPS	f_{CLK} = 2.048MHz
Common-mode Input Voltage	V_{CM}	AVSS+ 0.3	--	AVDD- 0.3	V	Set HDR_EN =1
		AVSS+ 0.3	--	AVDD- 1.3	V	Set HDR_EN =0
ADC DC performance						
Equivalent Input Noise (0.01 Hz ~ 70 Hz)		--	1.2	--	μVpp	1000 points, 4-second data, gain = 24, T_A =

						25°C, inputs shorted
Integral Nonlinearity (INL)	INL	--	14	--	PPM	V_{IN} = -3dBFs, gain=12
Offset Error		--	14	--	μV	gain = 12, 250 SPS
Offset Error Drift		--	80	--	nV/°C	
Gain Error		--	1.5	--	% of FS	gain = 12, 250 SPS
Gain Error Drift		--	3	--	PPM/℃	
Channel-to-Channel Gain Match		--	0.2	--	% of FS	
ADC AC performance						
Common Mode Rejection Ratio	CMRR	--	-120	--	dB	f_{CM} = 50Hz and 60Hz
Power Supply Rejection Ratio	PSRR	--	112	--	dB	f_{PS} = 50Hz and 60Hz
Crosstalk		--	-110	--	dB	f_{IN} = 50Hz and 60Hz, gain=12
Signal-to-Noise Ratio	SNR	--	113	--	dB	V_{IN} = -6dBFs, f_{IN} = 10Hz, gain=12
Total Harmonic Distortion	THD	--	-98	--	dB	V_{IN} = -6dBFs, f_{IN} = 60Hz, gain=12
Body BIAS Amplifier						
Noise		--	2	--	uVrms	BW = 150 Hz
Gain-Bandwidth Product	GBW	--	100	--	kHz	50-k Ω || 10-pF load, gain = 1
Slew Rate	SR	--	0.07	--	V/μs	50-k Ω || 10-pF load, gain = 1
Total Harmonic Distortion	THD	--	-80	--	dB	f_{IN} = 10Hz, gain = 1
Output Short-Circuit Current	ISC	--	1.1	--	mA	
Quiescent Power Consumption		--	20	--	μA	
Electrode Drop Detection						
AC Detection Selectable Frequency		--	f_{DR}/4	--	Hz	Continuous Detection
		--	DR/4, 7.8 ,	--		Periodic Detection

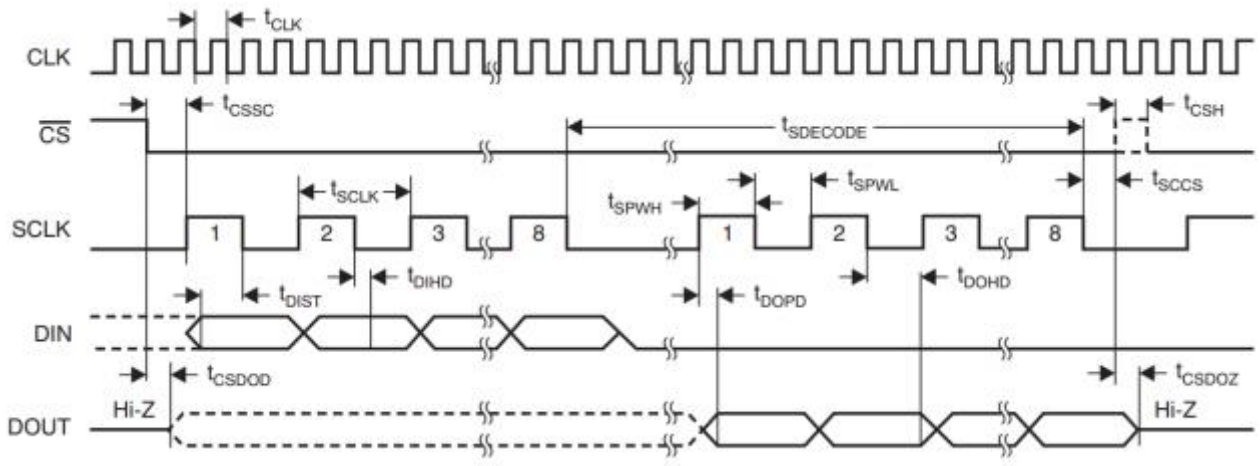
			31.2			
Constant Current Source Current		--	10	--	nA	ILEAD_OFF[1:0] = 00
		--	40	--		ILEAD_OFF[1:0] = 01
		--	8.5	--	µA	ILEAD_OFF[1:0] = 10
		--	34	--		ILEAD_OFF[1:0] = 11
Constant Current Source Accuracy		--	20%	--		
Comparator Threshold Accuracy		--	±30	--	mV	
External Reference						
Input Resistance		--	6.9	--	kΩ	
Internal Reference						
Internal Reference Voltage	V_{REF}	--	4.6	--	V	
V_{REF} Accuracy		--	±0.4%	--		
V_{REF} Temperature Drift		--	35	--	ppm/°C	
V_{REF} Start-up Time		--	25	--	ms	
System Monitoring						
Analog Supply Measurement Error		--	2%	--		
Digital Supply Measurement		--	2%	--		
Device Wake-up		--	150	--	ms	From power-up to DRDY low
		--	31.25	--	µs	STANDBY mode
Temperature Measurement						
Voltage		--	145	--	mV	TA = 25°C
Conversion Factor		--	490	--	µV/°C	
Test Signal						
Frequency		f_{CLK} / 2 21 , f_{CLK} / 2 20			Hz	
Voltage		1 * V_{REF} / 2400 , 2 * V_{REF} / 2400			V	
Voltage Accuracy		±2%				
Clock						

Internal Clock Frequency		--	2.048	--	MHz	
Internal Clock Accuracy		--	--	0.5%		TA = 25°C
		--	--	2.5%		TA = -40°C ~ +85°C
Internal Clock Start-up Time		--	20	--	μs	
Internal Clock Power Consumption		--	120	--	μW	
Digital Signal Level(DVDD=1.8V to 3.3V)						
High-Level Input	V_{IH}	0.8*DVDD	--	DVDD +0.1	V	
Low-Level Input	V_{IL}	-0.1	--	0.2*DVDD		
High-Level Output	V_{OH}	0.9*DVDD	--	--	V	
Low-Level Output	V_{OL}	--	--	0.1*DVDD	V	
Input Current		-10	--	10	μA	
Power Consumption(AVDD-AVSS=5V，DVDD=3.3V)						
AVDD Current	I_{AVDD}	--	2.3	--	mA	Internal reference enabled, 5V, HDR_EN=0
AVDD Current	I_{AVDD}	--	3.0	--	mA	Internal reference enabled, 5V, HDR_EN=1
DVDD Current	I_{DVDD}	--	0.7	--	mA	Normal Mode , DVDD=3.3V
Power Consumption		--	13.8	--	mW	Normal Mode (HDR_EN=0)
		--	17.3	--	mW	Normal Mode (HDR_EN=1)
		--	3.63	--	mW	Standby Mode, internal reference enabled
		--	14	--	μW	PWDN_=0 Mode

Serial Communication Timing

T_A = 25℃ unless otherwise specified

Parameter		2.7V≤DVDD≤3.6V		1.65V≤DVDD≤2V		Unit
		Min	Max	Min	Max	
t_{CLK}	Master clock period	414	514	414	514	ns
t_{CSSC}	CS low to first SCLK, setup time	6	--	17	--	ns
t_{SCLK}	SCLK period	50	--	66.6	--	ns
$t_{SPWH,L}$	SCLK pulse width, high and low	15	--	25	--	ns
t_{DIST}	DIN valid to SCLK falling edge: setup time	10	--	10	--	ns
t_{DIHD}	DIN valid after SCLK falling edge: hold time	10	--	11	--	ns
t_{CSH}	CS high pulse	2	--	2	--	t_{CLK}
t_{SCCS}	8th SCLK falling edge to CS high	4	--	4	--	t_{CLK}
$t_{SDECODE}$	Command decode time	4	--	4	--	t_{CLK}
$t_{DISCK2ST}$	DAISY_IN valid to SCLK rising edge: setup time	10	--	10	--	ns
$T_{DISCK2HT}$	DAISY_IN valid after SCLK rising edge: hold time	10	--	10	--	ns
t_{DOHD}	SCLK falling edge to DOUT invalid: hold time	10	--	10	--	ns
t_{DOPD}	SCLK rising edge to DOUT valid: setup time	--	17	--	32	ns
t_{CSDOD}	CS low to DOUT driven	10	--	20	--	ns
t_{CSDOZ}	CS high to DOUT to Hi-Z	--	17	--	20	ns

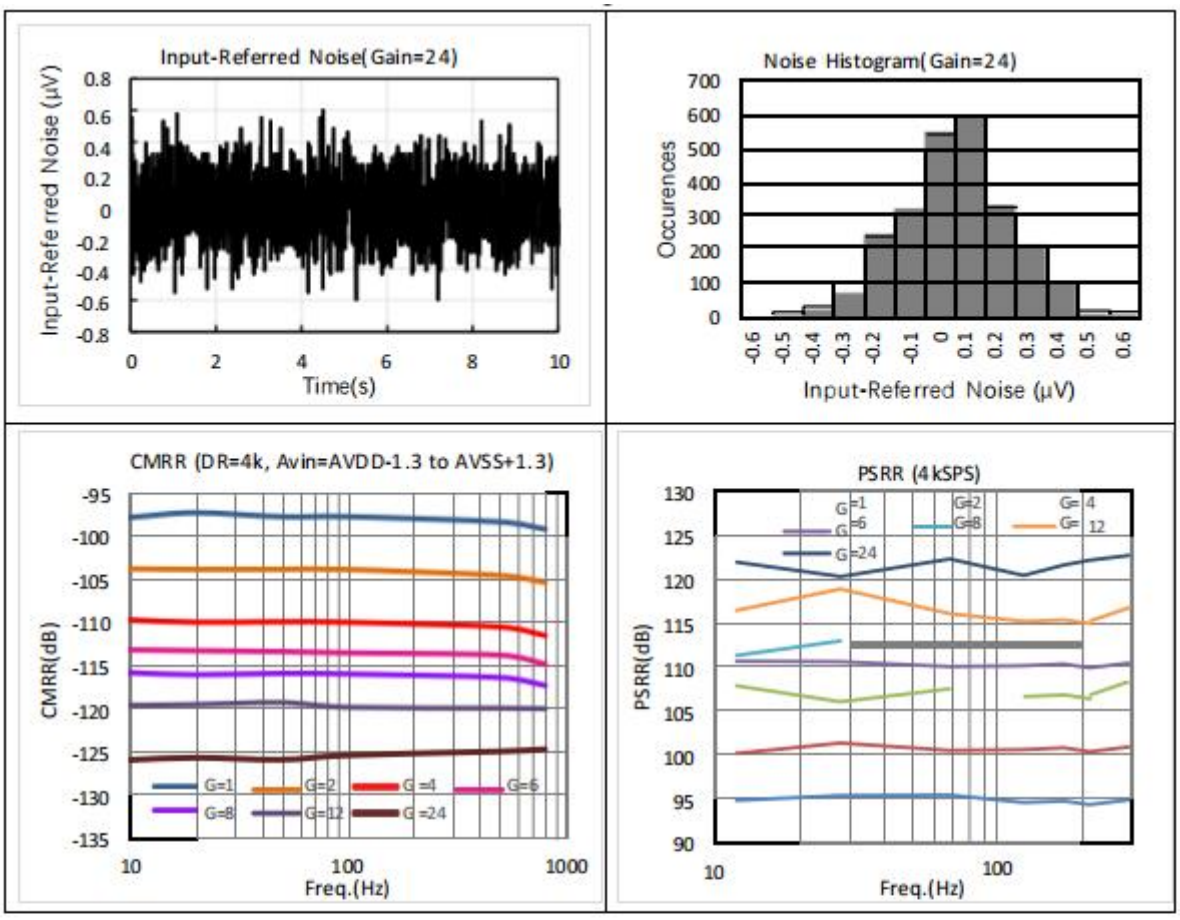


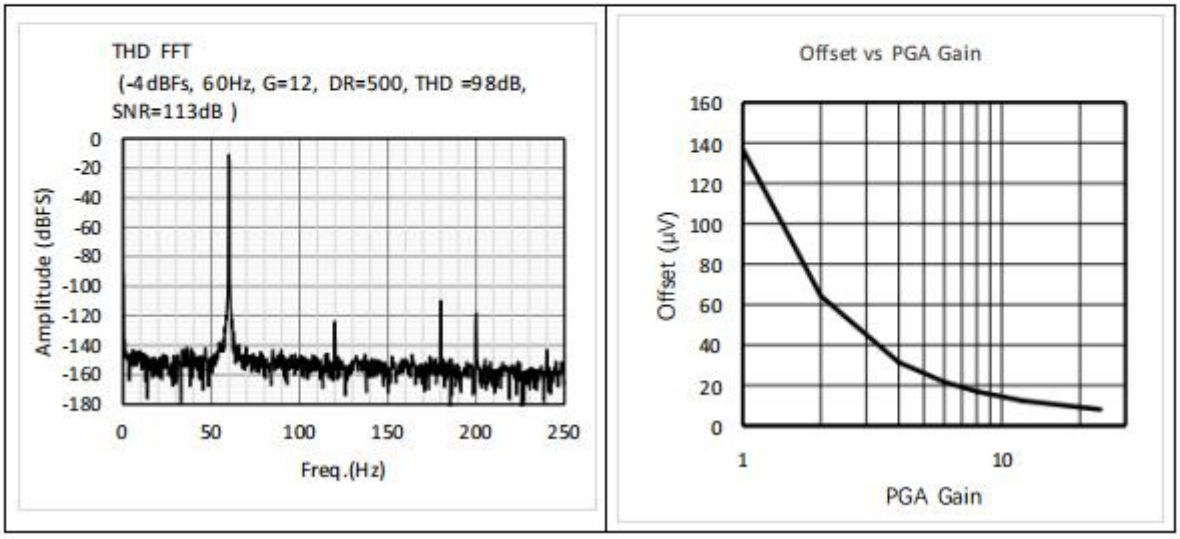
Serial Communication Timing Diagram

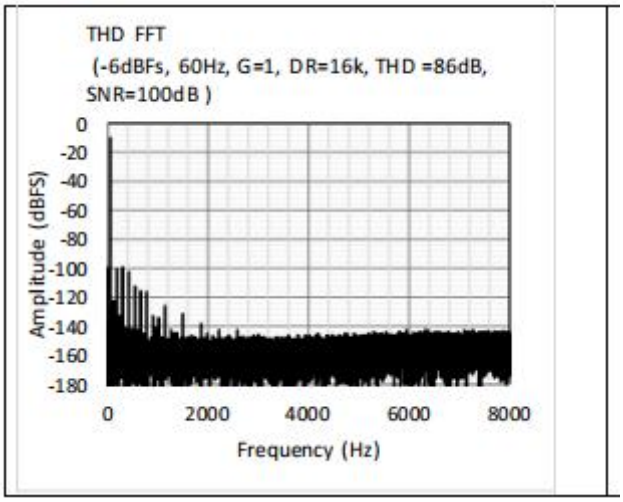
Note: SPI is configured as CPOL=0 and CPHA=1.

Typical Characteristics

All electrical parameters are measured at:T_A = 25℃, AVDD - AVSS = 5V, DVDD = 3.3V, V_{REF} = 4.63V,external clock f_{CLK} = 2.048MHz, data rate = 250SPS, gain = 12,unless otherwise noted.







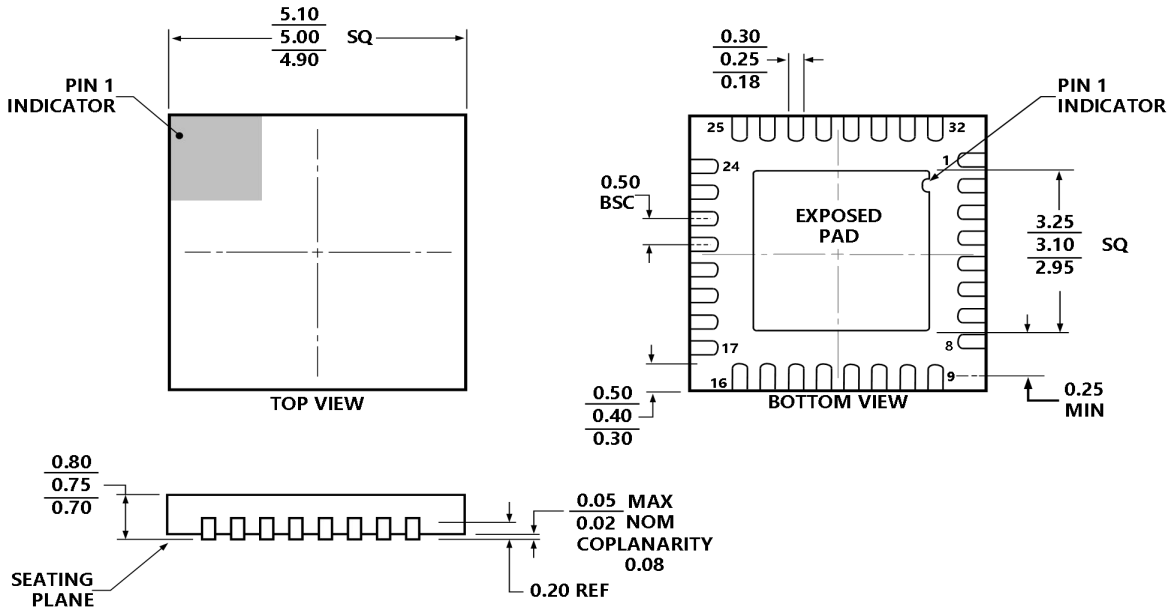
Register Map

Address	Register Name	Default Settings	Register Bit							
			7	6	5	4	3	2	1	0
Read-only ID Register										
00h	ID	xxh	REV_ID[2:0]							
Global Settings Across Channels										
01h	CONFIG 1	96h	1	DAISY_ EN_	CLK_EN	1	HDR_E N	DR[2:0]		
02h	CONFIG 2	00h	1	1	0	INT_CA L	0	CAL_A MP0	CAL_FREQ[1:0]	
03h	CONFIG 3	60h	PD_REF BUF_	1	VREF_4 V	BIAS_M EAS	BIASRE F_INT	PD_BIA S_	BIAS_L OFF_SE NS	BIAS_ST AT
04h	LOFF	00h	COMP_TH[2:0]							
Channel-Specific Settings										
05h	CH1SET	61h	PD1	GAIN1[2:0]			SRB2	MUX1[2:0]		
06h	CH2SET	61h	PD2	GAIN2[2:0]			SRB2	MUX2[2:0]		
0Dh	BIAS_SE NSP	00h								
0Eh	BIAS_SE NSN	00h								
0Fh	LOFF_SE	00h								

	NSP									
10h	LOFF_SENSN	00h								
11h	LOFF_FLIP	00h								
Lead Open Status Register (Read-only)										
12h	LOFF_STATP	00h							IN2P_OFF	IN1P_OFF
13h	LOFF_STATN	00h							IN2N_OFF	IN1N_OFF
GPIO and Other Registers										
14h	GPIO	0Fh	GPIOD[4:1]				GPIOC[4:1]			
15h	PACE	00h	0	0	SRB1	0	0	PACE_SEL		PD_PACE_b
16h	RESP	00h	RESP_DEMOD_EN	RESP_MOD_EN	0	RES_PH			RESP_CTRL	
17h	CONFIG4	00h	0	0	0	0	SINGLE_SHOT	0	PD_LOFF_COMP_	0

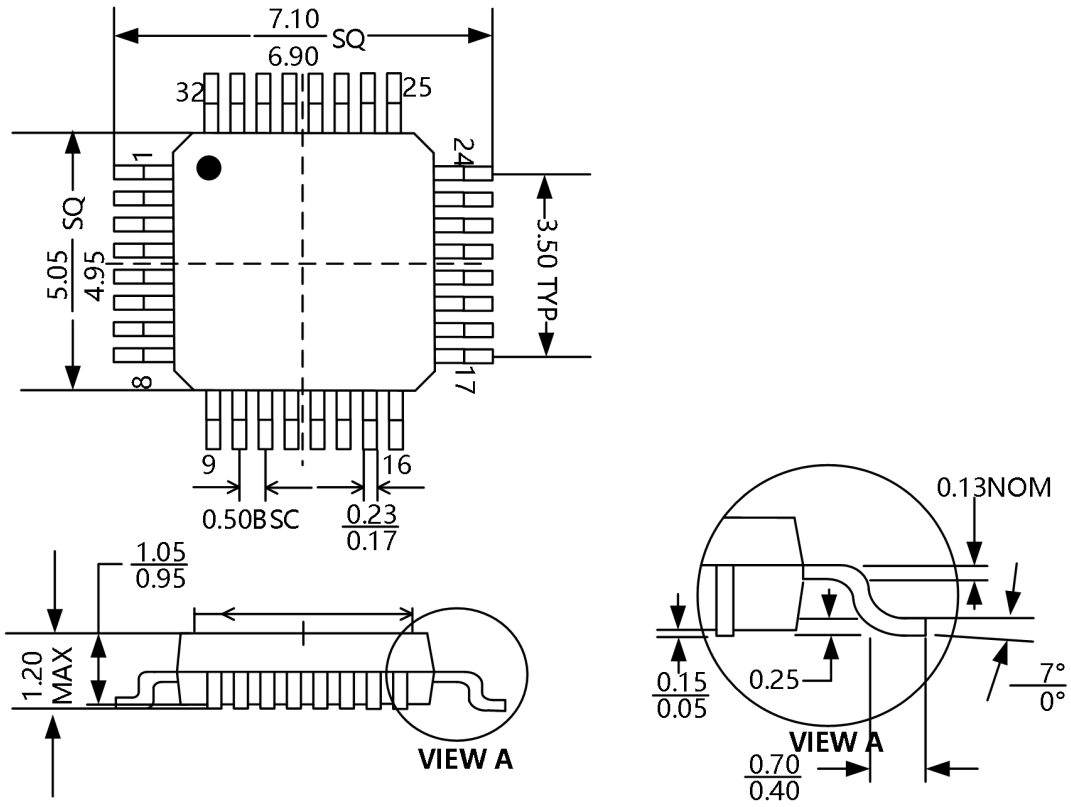
Package Outline and Dimensions

VQFN-32



VQFN-32 Package Drawing

TQFP-32



TQFP-32 Package Drawing

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION	MAKING INFORMATION
CBM24AD92-2CQ		-40℃~85℃	VQFN-32		Tray，490
CBM24AD92-2CQP		-40℃~85℃	TQFP-32		