Features

- Low power (full operating conditions): 1.0 W @ 1 GSPS, 600mW @ 500 MSPS
- Single carrier WCDMA ACLR:80dBc @ 80 MHz IF
- Adjustable analog output: 8.7 mA-31.7 mA (R_L = 25 Ω to 50 Ω)
- Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth
- Auxiliary DACs allow control of external VGA and offset control
- Multiple chip synchronization interface
- High performance, low noise PLL clock multiplier
- Digital Inverse Sinc Filter
- 100-lead Exposed Paddle TQFP Package

Applications

- Wireless infrastructure: W-CDMA, GSM, CDMA2000, TD-SCDMA, WiMax, LTE
- Digital high or low IF synthesis
- Internal digital up conversion capability
- Transmit diversity
- Wideband communications: LMDS/MMDS, point-to-point

General Description

The CBM97D79TQ is dual, 16-bit, high dynamic range, digital-to-analog converters (DACs) that provide a sample rate of 1 GSPS, permitting multicarrier generation up to the Nyquist frequency. They include features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the ADL537XFMOD Series modulator made by ADI company. The three-wire interface provides for programming and readback of many internal parameters. Full-scale output current can be programmed over a range of 10 mA to 30 mA. The devices are manufactured on an advanced 0.18μm CMOS process and operate on 1.8 V and 3.3 V supplies for a total power consumption of 1.0W.

The CBM97D79TQ can be functionally divided into digital filter unit, DAC core unit, clock (including internal PLL) unit, auxiliary DAC, multi-chip synchronization unit, etc. The digital part performs digital interpolation, digital domain real modulation and complex modulation on the input signal. The DAC core converts the digital signal from digital to analog. SPI configures all of the chip. The clock unit provides high-quality clock for the circuit, four auxiliary DACs are used

for channel gain and offset correction, The multi-chip synchronization unit is responsible for the synchronization function between multiple chips.

CATALOG

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Functional Block Diagram

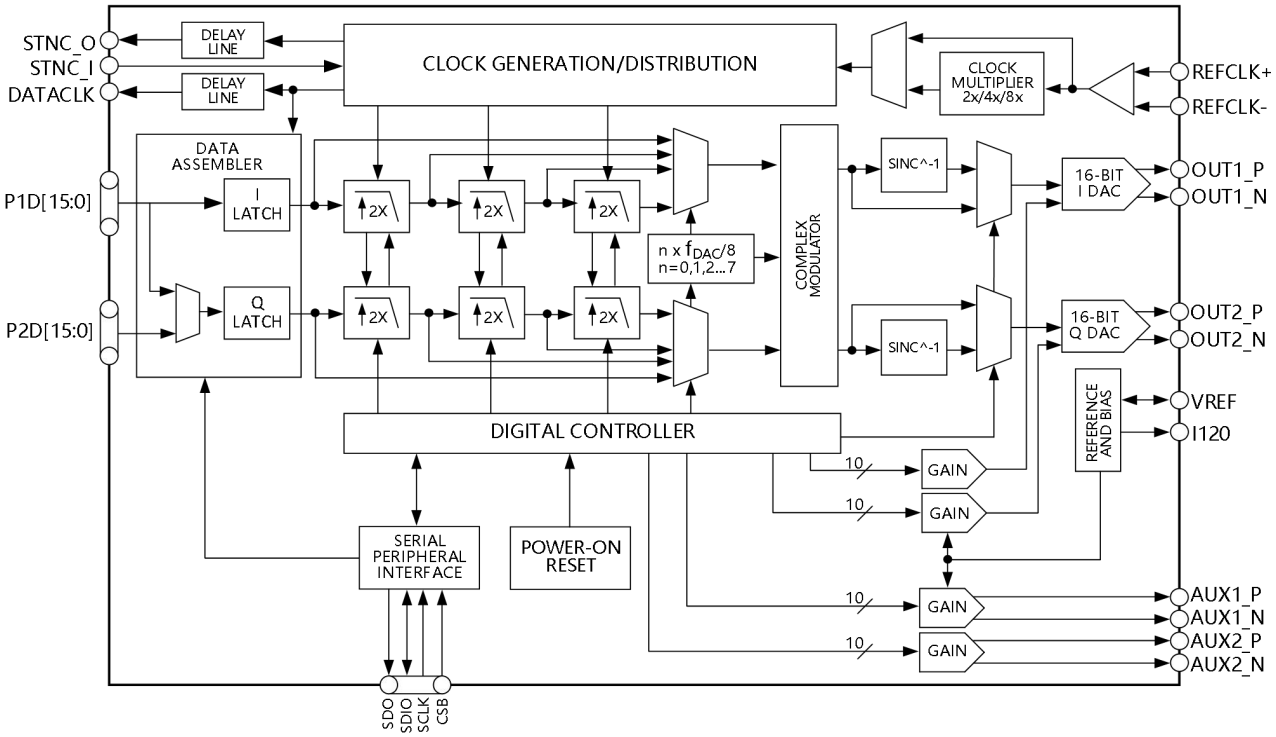
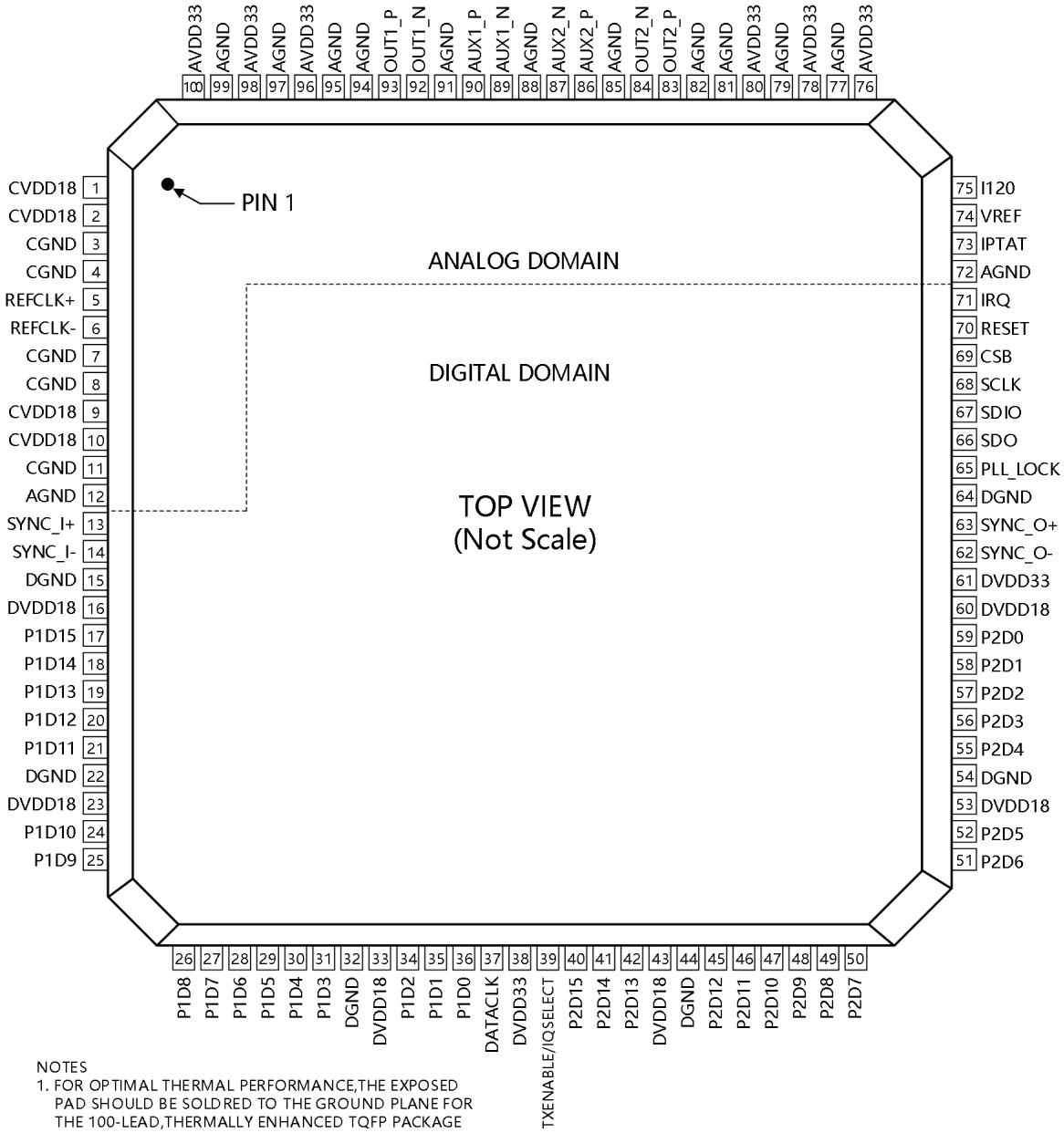


Figure 1. Functional Block Diagram

Pin Arrangement Diagram



NOTES
1. FOR OPTIMAL THERMAL PERFORMANCE,THE EXPOSED PAD SHOULD BE SOLDRED TO THE GROUND PLANE FOR THE 100-LEAD,THERMALLY ENHANCED TQFP PACKAGE

Figure 2. Pin Arrangement Diagram

Pin Descriptions

Pin No.	Pin Name	Pin Describe	Pin No.	Pin Name	Pin Describe
1	CVDD18	1.8 V Clock Supply.	32	DGND	Digital Common.
2	CVDD18	1.8 V Clock Supply.	33	DVDD18	1.8 V Digital Supply.
3	CGND	Clock Common.	34	P1D2	Port 1, Data Input D2.
4	CGND	Clock Common.	35	P1D1	Port 1, Data Input D1
5	REFCLK+	Differential Clock Input.	36	P1D0	Port 1, Data Input D0(LSB)
6	REFCLK−	Differential Clock Input.	37	DATACLK	Data Clock Output.
7	CGND	Clock Common.	38	DVDD33	3.3 V Digital Supply.
8	CGND	Clock Common.	39	TXENABLE/ IQSELECT	Transmit Enable. In single port mode, the pin can used to be IQSELECT also.
9	CVDD18	1.8 V Clock Supply.			
10	CVDD18	1.8 V Clock Supply.	40	P2D15	Port 2, Data Input D15 (MSB)
11	CGND	Clock Common.	41	P2D14	Port 2, Data Input D14
12	AGND	Analog Common.	42	P2D13	Port 2, Data Input D13
13	SYNC_I+	Differential Synchronization Input.	43	DVDD18	1.8 V Digital Supply.
14	SYNC_I−	Differential Synchronization Input.	44	DGND	Digital Common.
15	DGND	Digital Common.	45	P2D12	Port 2, Data Input D12
16	DVDD18	1.8 V Digital Supply.	46	P2D11	Port 2, Data Input D11
17	P1D15	Port 1, Data Input D15 (MSB).	47	P2D10	Port 2, Data Input D10
18	P1D14	Port 1, Data Input D14.	48	P2D9	Port 2, Data Input D9
19	P1D13	Port 1, Data Input D13.	49	P2D8	Port 2, Data Input D8
20	P1D12	Port 1, Data Input D12.	50	P2D7	Port 2, Data Input D7
21	P1D11	Port 1, Data Input D11.	51	P2D6	Port 2, Data Input D6
22	DGND	Digital Common.	52	P2D5	Port 2, Data Input D5
23	DVDD18	1.8 V Digital Supply.	53	DVDD18	1.8 V Digital Supply.
24	P1D10	Port 1, Data Input D10	54	DGND	Digital Common.
25	P1D9	Port 1, Data Input D9	55	P2D4	Port 2, Data Input D4
26	P1D8	Port 1, Data Input D8	56	P2D3	Port 2, Data Input D3
27	P1D7	Port 1, Data Input D7	57	P2D2	Port 2, Data Input D2
28	P1D6	Port 1, Data Input D6	58	P2D1	Port 2, Data Input D1

29	P1D5	Port 1, Data Input D5	59	P2D0	Port 2, Data Input D0（LSB）
30	P1D4	Port 1, Data Input D4	60	DVDD18	1.8 V Digital Supply.
31	P1D3	Port 1, Data Input D3	61	DVDD33	3.3 V Digital Supply.
62	SYNC_O−	Differential Synchronization Output.	80	AVDD33	3.3 V Analog Supply.
63	SYNC_O+	Differential Synchronization Output.	81	AGND	Analog Common.
64	DGND	Digital Common.	82	AGND	Differential DAC Current Output, Channel 2.
65	PLL_LOCK	PLL Lock Indicator.	83	OUT2_P	Differential DAC Current Output, Channel 2.
66	SDO	Port Data Output.	84	OUT2_N	Analog Common.
67	SDIO	SPI Port Data Input/Output.	85	AGND	Analog Common.
68	SCLK	SPI Port Clock.	86	AUX2_P	Auxiliary DAC Current Output, Channel 2.
69	CSB	SPI Port Chip Select Bar.	87	AUX2_N	Auxiliary DAC Current Output, Channel 2.
70	RESET	Reset, Active High.	88	AGND	Analog Common.
71	IRQ	Interrupt Request.	89	AUX1_N	Auxiliary DAC Current Output, Channel 1.
72	AGND	Analog Common.	90	AUX1_P	Auxiliary DAC Current Output, Channel 1.
73	IPTAT	Factory Test Pin. Output current is proportional to absolute temperature, approximately 14μA at 25°C with approximately 20 nA/°C slope. This pin should remain floating.	91	AGND	Analog Common.
			92	OUT1_N	Differential DAC Current Output, Channel 1.
			93	OUT1_P	Differential DAC Current Output, Channel 1.
			94	AGND	Analog Common.
74	VREF	Voltage Reference Output.	95	AGND	Analog Common.
75	I120	120μA Reference Current.	96	AVDD33	3.3 V Analog Supply.
76	AVDD33	3.3 V Analog Supply.	97	AGND	Analog Common.
77	AGND	Analog Common.	98	AVDD33	3.3 V Analog Supply.
78	AVDD33	3.3V Analog Supply.	99	AGND	Analog Common.
79	AGND	3.3V Analog Common	100	AVDD33	3.3 V Analog Supply.

Recommended Operating Conditions

- Supply Voltage: 3.3V,1.8V
- Operating Temperature: -40℃～85℃

Absolute Maximum Ratings

- Supply Voltage: -0.3V~V_{DD}+0.3V (1.8V voltage correspond to V_{DD} = 1.8V, 3.3V voltage correspond to V_{DD} = 3.3V)
- Storage Temperature(T_S): - 65℃～150℃

Typical Test Results

In order to evaluate the chip, the dynamic and static parameters of various operation modes of the chip are tested at normal atmospheric temperature. The dynamic parameters mainly include spurious free dynamic range and third-order intermodulation distortion. Static parameters include the test of differential nonlinearity and integral nonlinearity

1. Dynamic performance test

(1) Spurious free dynamic range (SFDR)

Table 1 show the test result of spurious free dynamic range of the ship (patch test) under various working modes. The result represents the test value that measured in either case that external signal is direct input into conversion clock and internal open PLL.At the table 1, in the case of f_{dac}=100MSPS, f_{out}=20MHz, the PLL not on. This case led to V_{CO} of PLL could not provide the conversion frequency (The same is true for ADI primary products).

Table 1. Test value of spurious free dynamic range

spurious free dynamic range (SFDR)	test condition	Test value (External clock)	Test value (Internal phase locked loop)
f_{dac}=100SPS, f_{out}=20MHz	The filter is 1x mode, No offset, no modulation	84dBc	none
f_{dac}=200SPS, f_{out}=50MHz	The filter is 1x mode, No offset, no modulation	90dBc	88dBc
f_{dac}=400SPS, f_{out}=70MHz	The filter is 2x mode, No offset, no modulation	75dBc	75dBc
f_{dac}=800SPS, f_{out}=70MHz	The filter is 4x mode, No offset, no modulation	76dBc	76dBc
f_{dac}=1000SPS, f_{out}=10MHz	The filter is 8x mode, No offset, no modulation	73dBc	72dBc
f_{dac}=1000SPS, f_{out}=40MHz	The filter is 8x mode, No offset, no modulation	85dBc	83dBc

Figure 3 show the test value of spurious free dynamic range at the conversion rate 800MSPS and If output that frequency is 70MHz.The measurement results of channel I are shown in the figure.

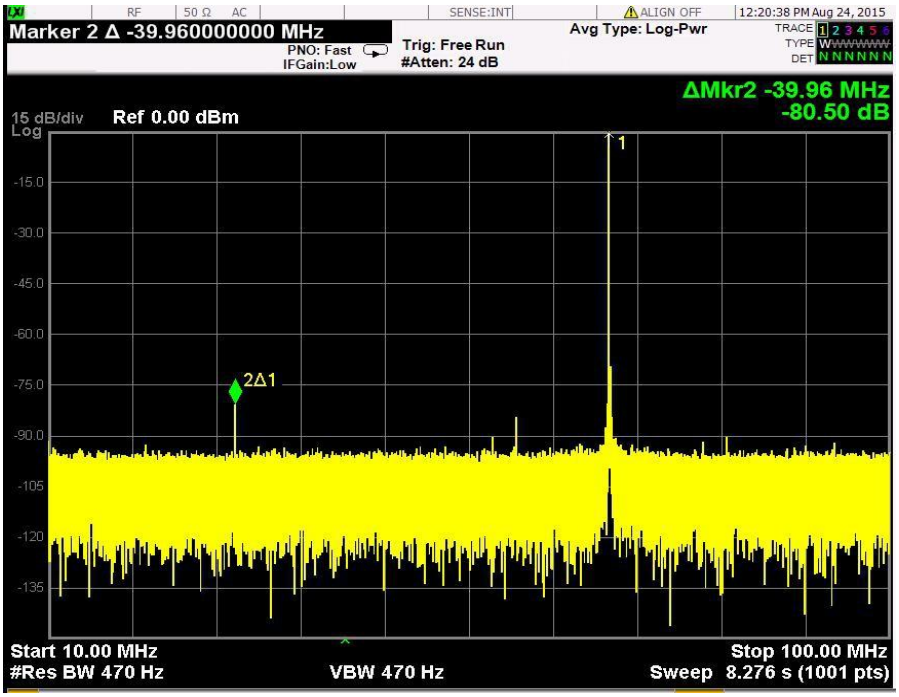


Figure 3. Test value of spurious free dynamic range (If output 70MHz, Conversion rate 800MSPS)

(2) Third order intermodulation distortion (IMD)

Table 2 show the test result of third order intermodulation distortion of the ship (patch test) under various working modes.

Table 2. Test result of third order intermodulation distortion

spurious free dynamic range (SFDR)	test condition	Test value (External clock)	Test value (Internal phase locked loop)
f_{dac}=200SPS, f_{out}=20MHz	The filter is 1x mode, No offset, no modulation	79dBc	76dBc
f_{dac}=400SPS, f_{out}=50MHz	The filter is 1x mode, No offset, no modulation	76dBc	80dBc
f_{dac}=400SPS, f_{out}=70MHz	The filter is 2x mode, No offset, no modulation	73dBc	75dBc
f_{dac}=800SPS, f_{out}=70MHz	The filter is 4x mode, offset f_{data}, no modulation	73dBc	67dBc

Figure 4 show the test value of third order intermodulation distortion at the conversion rate 400MSPS and If output that frequency is 70MHz or 80MHz. The measurement results of channel I are shown in the figure.

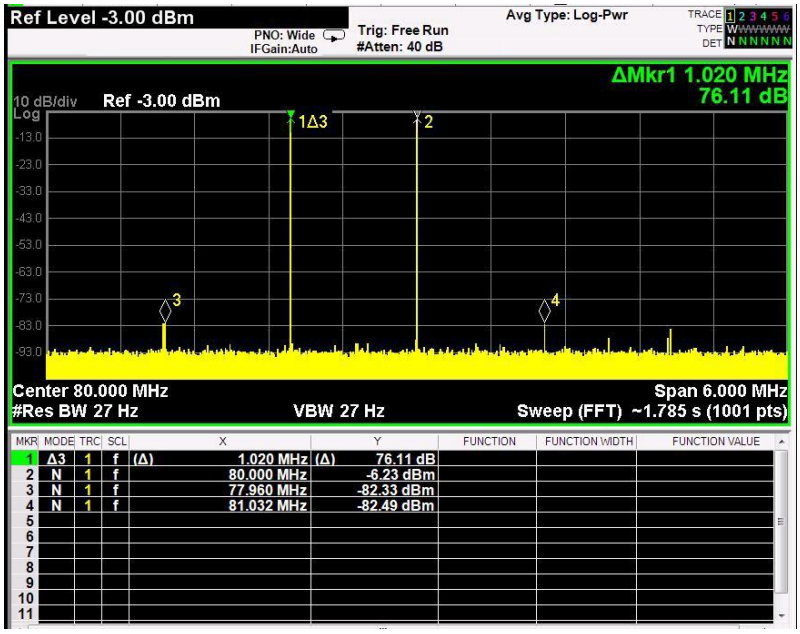


Figure 4. Test value of third order intermodulation distortion (If output 79MHz or 80MHz, Conversion rate 400MSPS)

2. Static Testing

Table 3. Test value of chip static parameters

Chip number	Circuit	Differential nonlinearity (LSB)	Integral nonlinearity (LSB)	Offset error (%FSR)	Gain error (%FSR)
1	I	-0.61~2.72	-2.34~5.45	0.003%	-1.60%
	Q	-1.14~1.75	-2.47~3.85	0.004%	-1.60%
2	I	-1.86~1.28	-3.08~3.24	0.003%	-1.80%
	Q	-2.55~1.81	-6.85~2.76	0.004%	-1.80%
3	I	-2.69~1.33	-2.41~4.04	0.003%	-1.60%
	Q	-3.62~0.08	-2.84~2.96	0.004%	-1.60%
4	I	-2.63~0.76	-5.18~1.51	0.003%	-2.20%
	Q	-2.16~1.59	-3.49~3.29	0.004%	-2.20%
5	I	-1.75~2.16	-4.08~4.37	0.002%	-1.60%
	Q	-2.74~0.814	-2.69~4.33	0.003%	-1.60%

Table 3 show the test value of Randomly selected five chip static testing.

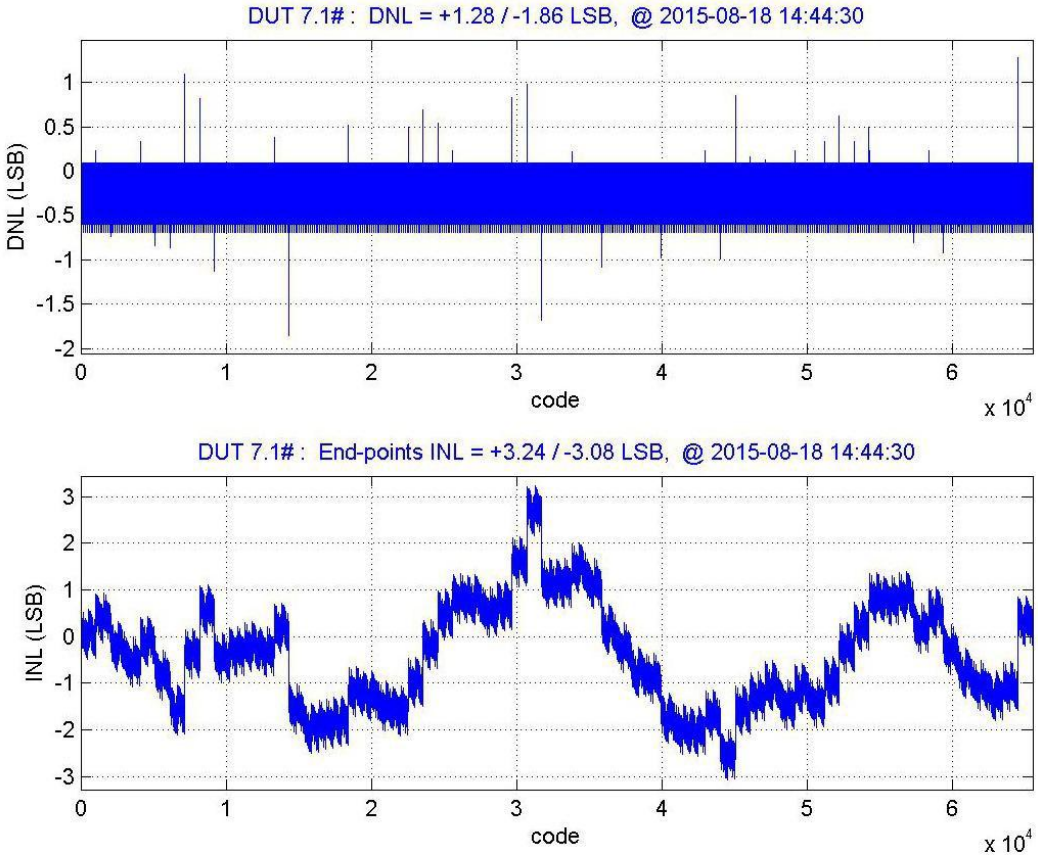
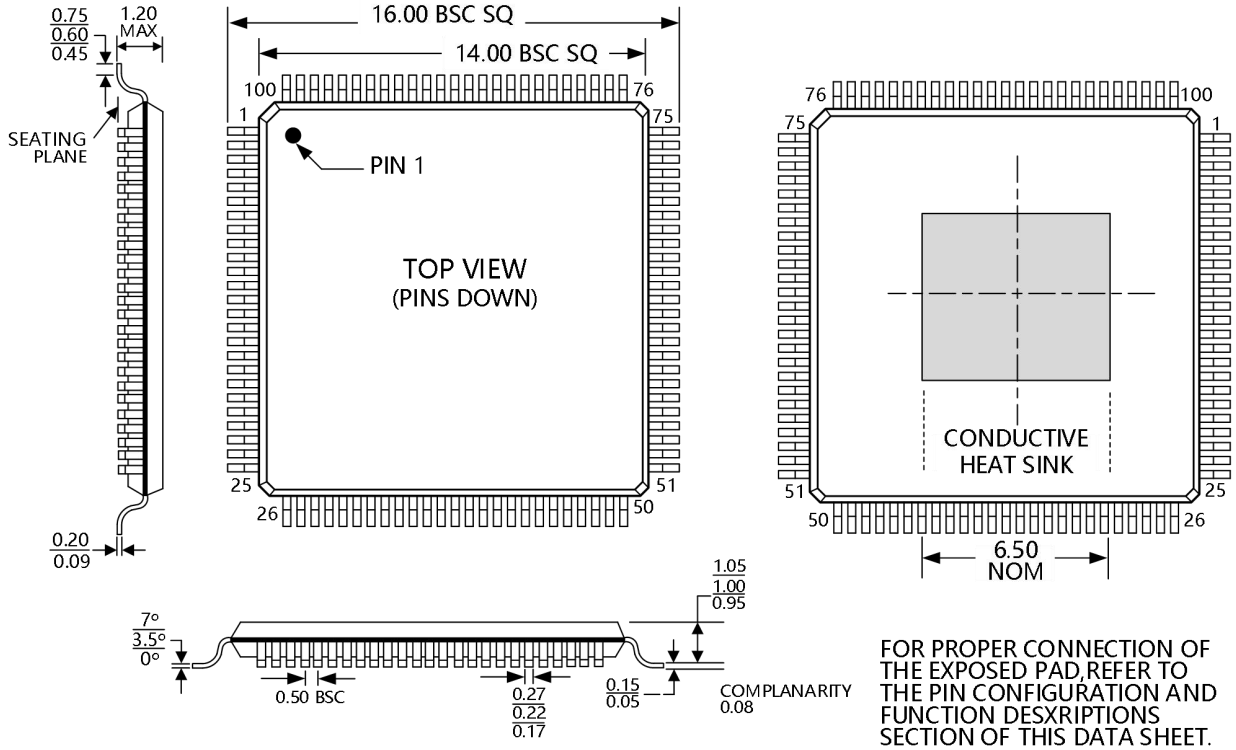


Figure 5. Typical differential nonlinearity / integral nonlinearity diagram

Figure 5 show the measured figure of typical differential nonlinearity and integral nonlinearity.

Package Outline Dimensions



FOR PROPER CONNECTION OF THE EXPOSED PAD,REFER TO THE PIN CONFIGURATION AND FUNCTION DESXRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MS-026-AED-HDT

Unit: millimeter (mm)

Matters Need Attention

1. installation:

1) The shipshape ground is required for the circuit board of application object.

2) The application object should use multiwiring board including independence ground layer.

2. usage:

1) The digital grounding and analog grounding of circuit board of application object should be separated as far as possible, digital line can not arrange beside of analog line or under the ADC.

2) Input wires should be short as much as possible to minimize the input of parasitic capacitance and noise.

3) It is important that the ground of chip should be connected to the PCB through as many channels as possible and plentiful area.

3. protection:

Although all the terminations of circuit are designed ESD protection structure, high energy electric pulse may be damaged the circuit. Electrostatic protection should be paid attention d during the test, transport and keep in reserve.

Common Failure Treatment method

1. zero output signal: Checking whether the Power supply voltage, Input Signal or clock are correct loading.
2. overflow signal occurs: Checking whether reference circuit is normal operation and whether amplitude of input signal is OK.
3. the device is unstable: Checking the power for guaranteeing stability of supply voltage

Parameter product information table

Research or manufacturing Company		Domestic products(corebai)	Foreign products (ADI)
No. and name of Detailed specification		Detailed specification of CBM97D79TQ with dual, 16-bit, 1GSPS D/A converter	——
Product model (specification)		CBM97D79TQ	AD9779ABSVZRL
Electrical performance index	RESOLUTION	16bits	16bits
	Differential Nonlinearity (DNL)	-6LSB~6 LSB	±2.1LSB（Typ.）
	Integral Nonlinearity (INL)	-10LSB~10LSB	±6LSB（Typ.）
	Offset Error	-1%FSR~+1%FSR	-0.001%FSR~0.001%FSR
	DAC Offset error temperature coefficient	-300ppm FSR/℃~ 300ppm FSR/℃	0.04ppm FSR/℃（Typ.）
	Gain Error	-8%FSR~+8%FSR	±2%FSR (Typ.)
	DAC Offset error temperature coefficient	-800ppm FSR/℃~ 800ppm FSR/℃	100ppm FSR/℃ (Typ.)
	Internal reference voltage	1.0V~1.5V	1.2V（Typ.）
	Reference voltage temperature coefficient	-250ppm/℃~250ppm/℃	30ppm/℃ (Typ.)
	Internal reference output resistance	3.5kΩ~7.5kΩ	5KΩ（Typ.）
	Full scale output current	7.5mA~32.5mA	8.66mA~31.66mA
	Output voltage compliance range	-1V~1V	-1.0V~1.0V
	Main DAC output resistance	Design assurance	10MΩ（Typ.）
	Monotonicity of main DAC output	Design assurance	Design assurance
	Auxiliary DAC output resolution	Design assurance	10 位
	Auxiliary DAC output resistance	Design assurance	1MΩ（Typ.）
	Auxiliary DAC output monotonicity	Design assurance	Design assurance
	Auxiliary DAC full scale output current	-2.5mA~2.5mA	-1.998mA~1.998mA
	Auxiliary DAC output voltage range (source)	0V~1.6V	0V~1.6V
	Auxiliary DAC output voltage range (suction)	0.8V~1.6V	0.8V~1.6V
	Analog supply voltage (V_{DDA})	3.13V~3.47V	3.13V~3.47V
	Analog supply voltage (V_{DDC})	1.7V~2.05V	1.7V~2.05V
	Digital power supply voltage (V_{DDD}<3.3>)	3.13V~3. 47V	3.13V~3. 47V
	数字电源电压Digital power supply voltage (V_{DDD}<1.8>)	1.7V~2.05V	1.7V~2.05V

	power waste（1X mode, f_{DAC}=100MSPS，IF=1MHz)	--	≤300mW（Typ.）
	power waste(2X mode, f_{DAC}=320MSPS IF=16MHz，PLL close)	≤650mW	498mW（Typ.）
	1×Mode delay	Design assurance	25个DACCLK cycle (Typ.)
	2×Mode delay	Design assurance	70个DACCLK cycle Typ.)
	4×Mode delay	Design assurance	146个DACCLK cycle (Typ.)
	8×Mode delay	Design assurance	297个DACCLK cycle (Typ.)
	Anti SINC mode	Design assurance	18个DACCLK cycle (Typ.)
	Maximum clock rate of three wire interface	≥6MHz	≥40MHz
	Minimum width of clock high pulse	Design assurance	≥12.5ns
	Minimum width of clock low pulse	Design assurance	≥12.5ns
	SDIO setup time	Design assurance	≥2.8ns
	SDIO Hold time	Design assurance	≥0.0ns
	CSB setup time	Design assurance	≥2.8ns
	SDO Data validity time	Design assurance	≥2.0ns
	Power on time	Design assurance	260mS（Typ.）
	Minimum pulse width of reset signal	Design assurance	≤2 个 DACCLK
	Spurious free dynamic range (f_{DAC} =100MSPS,f_{out}=20MHz)	≥65dBc	82dBc（Typ.）
	Spurious free dynamic range (f_{DAC} =200MSPS,f_{out}=50MHz)	--	82dBc（Typ.）
	Spurious free dynamic range (f_{DAC} =400MSPS,f_{out}=70MHz)	--	80dBc（Typ.）
	Spurious free dynamic range (f_{DAC} =800MSPS,f_{out}=70MHz)	≥60dBc	87dBc（Typ.）
	dual-tone inter-modulation (f_{DAC} =200MSPS,f_{out}=50MHz)	≥65dBc	91dBc（Typ.）
	dual-tone inter-modulation (f_{DAC} =200MSPS,f_{out}=50MHz)	--	85dBc（Typ.）
	dual-tone inter-modulation (f_{DAC} =400MSPS,f_{out}=80MHz)	--	81dBc（Typ.）
	dual-tone inter-modulation (f_{DAC} =800MSPS,f_{out}=100MHz)	≥55dBc	81dBc（Typ.）
	Noise spectral density (f_{DAC} =200MSPS,f_{out}=80MHz)	--	-158dBm/Hz（Typ.）
	Noise spectral density (f_{DAC} =400MSPS,f_{out}=80MHz)	--	-160dBm/Hz（Typ.）
	Noise spectral density (f_{DAC} =800MSPS,f_{out}=80MHz)	--	-161dBm/Hz（Typ.）
	First critical channel leakage (f_{DAC} =491.52MSPS,f_{out}=100MHz)	--	79dBc（Typ.）
	First critical channel leakage	--	74dBc（Typ.）

	(f_{DAC} =491.52MSPS, $f$out=200MHz)		
	DAC Clock input common mode voltage	350mV~450mV	300mV~500mV
	working frequency	≥1000MHz	≥900MHz
	Maximum clock rate	≥200MHz	≥250MHz)
	Input data relative to DATACLK set time	Design assurance	≥3.0ns
	Input data relative to DATACLK holding time	Design assurance	≥-0.05ns
	Input data relative to REFCLK set time	Design assurance	≥-0.80ns
	Input data relative to REFCLK holding time	Design assurance	≥3.8ns
	Second critical channel leakage (f_{DAC} =491.52MSPS, $f$out=100MHz)	--	81dBc (Typ.)
	Second critical channel leakage (f_{DAC} =491.52MSPS, $f$out=200MHz)	--	78dBc (Typ.)
Environmental adaptability	operating temperature	-40℃~85℃	-40℃~85℃
	Storage temperature	-65℃~150℃	-65℃~150℃
	Frequency-sweep Vibration	Method of GJB548B-2005 2007 test condition A	——
	thermal shock	Method of GJB548B-2005 1011 test condition B, 15 cycles	——
	Mechanical impact	Method of GJB548B-2005 2002 test condition B	——
	Quality grade	industrial standards	industrial standards
Reference of foreign companies and materials		AD9434 data sheets for AD9434 of ADI company	——
Package Outline Dimensions		TQFP100 (16mm×16mm×1.2mm)	SV-100-(16mm×16mm×1.2mm)
Alternative recommendations		■direct replacement □ Effective replacement □ function replacemer	

Package/Ordering Information

MODEL	CHANNEL	ORDERING NUMBER	PACKAGE DESCRIPTION	PAKEAGE OPTION	MAKING INFORMATION
CBM97D79TQ		-45℃-85℃	TQFP-100	TRAY,90	