Features

- Sample rate: 5MSPS
- 18 Bit Resolution, lossless code
- Characteristic of AC and DC(Type):
  Dynamic Range: 96.5dB
  SNR: 95.5dB
- Spurious free dynamic range（SFDR）: 115dB
- Total harmonic distortion: -113dB
- Linearity Errors: ±2.0LSB(MAX)
- Differential error: ±0.99LSB(MAX)
- Low power consumption: 64.5mW
- Supply voltage: 1.8V/5.0V
- Range of differential analog input:
  Allow any input range of ±VREF（0V to +VREF）, MAX(VREF) = 5V, 4.096V~5V (Type)(Any range of input)
- SAR structure: No pipeline delay
- Interface of digital logic: 1.8V
- Interface of serial LVDS
- Range of operating temperature: -40℃ to +85℃
- 32 pin, QFN32 plastic packaging

Application

- system of digital imaging
- digital X-ray machine
- Medical digital tomography
- Infrared camera
- Gradient control of nuclear magnetic resonance examination（MRI）
- High precision data acquisition
- spectral analysis

Description

The CBM79AD60G of 18-bit A/D Converter (Analog-to-Digital Converter) with sampling of 5MSPS is successive-approximation, it includes A/D core of low power consumption and 18-bit high speed, clock generation circuit of interior switch, error correction circuit and universal serial bus(USB).At the rising edge of conversion control signal(CNV),The voltage difference between the device sample input port of IN+ and IN- is provided backward voltage signal which operating voltage range is 0V to VREF. All the conversion results of the device output through serial high speed LVDS interface. A/D converter available in QFN32 packages, recommended operating temperature range is from -40℃~ to 85℃.

Catalog

Block Diagram

The block diagram of 18-bit A/D convert with sampling of 5MSps is shown in Figure 1

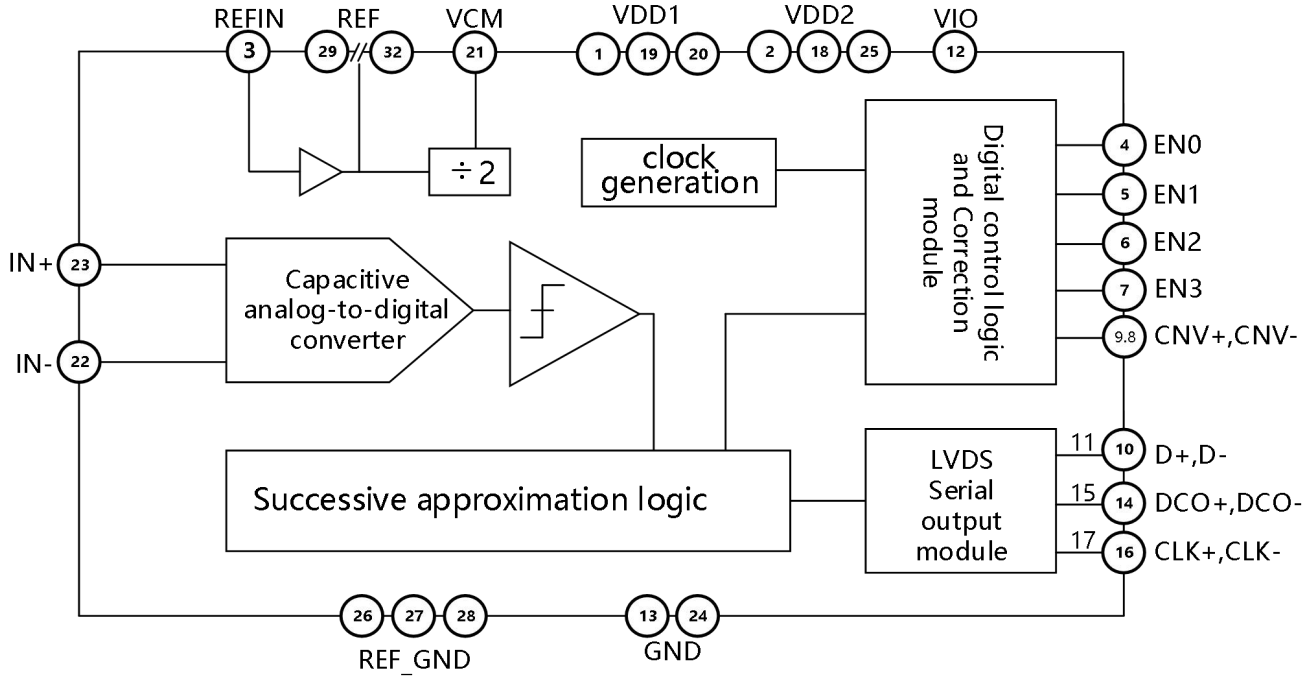


Figure 1. Block Diagram

Timing Sequence Diagram

Recommended timing sequence of operating 18-bit A/D convert with sampling of 5MSps is shown in Figure 2

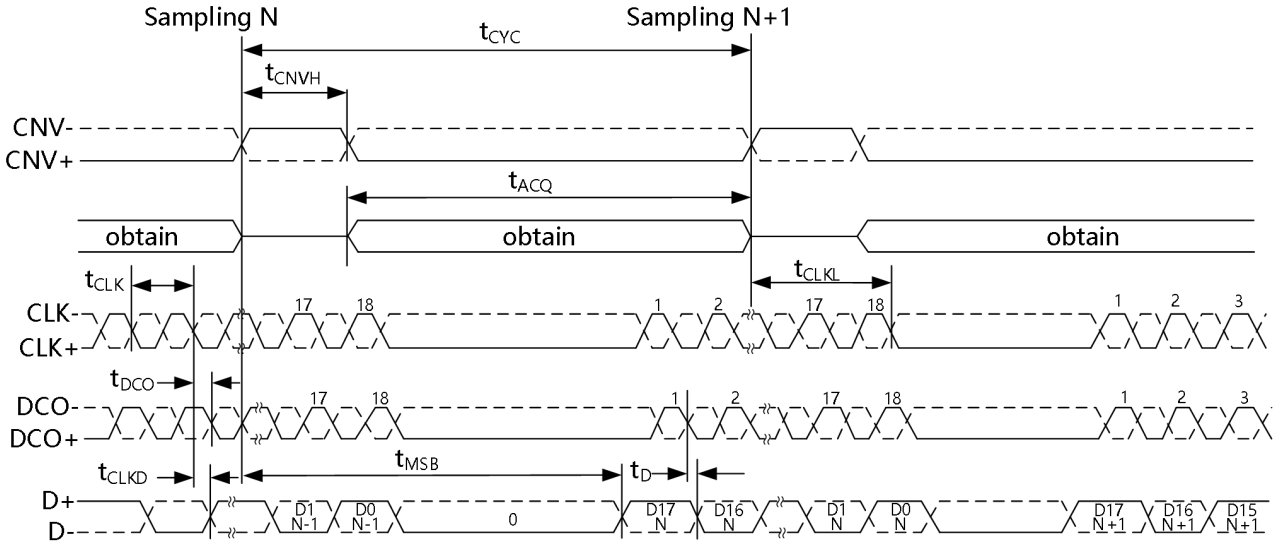


Figure 2. timing cycle of convert start and data output

Functional Block Diagram and Timing Characteristics

The control part logical combination of CBM79D60G of 18-bit A/D converter as followed table:

EN3	EN2	EN1	EN0	REFIN	describe of reference voltage mode
X	0	0	0	X	Power down mode, all current is off including LVS interface.
X	0	0	1	0V	LVDS interface Power on, interior reference voltage disabled, 5V external reference with sampling bandwidth of 28MHz (Recommended operational mode)
X	0	0	1	2.048V	internal reference enables, external voltage of 2.048V, REF provides 5V supply voltage, sampling bandwidth is 9MHz
X	0	1	0	0V	Internal reference voltage disabled, 4.096V external reference with sampling bandwidth of 28MHz
X	0	1	1	0V	sleep mode
0	1	0	0	X	LVDS test code output
1	1	0	0	X	Normal operation is invalid
X	1	0	1	0V	Internal reference voltage disabled, 5V external reference with sampling bandwidth of 9MHz
X	1	0	1	2.048V	internal reference enable, external voltage of 2.048V, REF provides 5V supply voltage, sampling bandwidth is 9MHz

X	1	1	0	0V	internal reference voltage disabled, 4.096V external reference with sampling bandwidth of 9MHz
X	1	1	1	0V	sleep mode
Note1: X indicate independent bit,AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DO = digital output; P = power. Note2: EN2 = 0 sets the 28 MHz of input bandwidth, and EN2 = 1 sets the 9 MHz of input bandwidth. EN3 = 1 enables the VCM reference output.					

Package Outline Dimensions

Package outline drawing of 18-bit A/D converter is shown in Figure 3

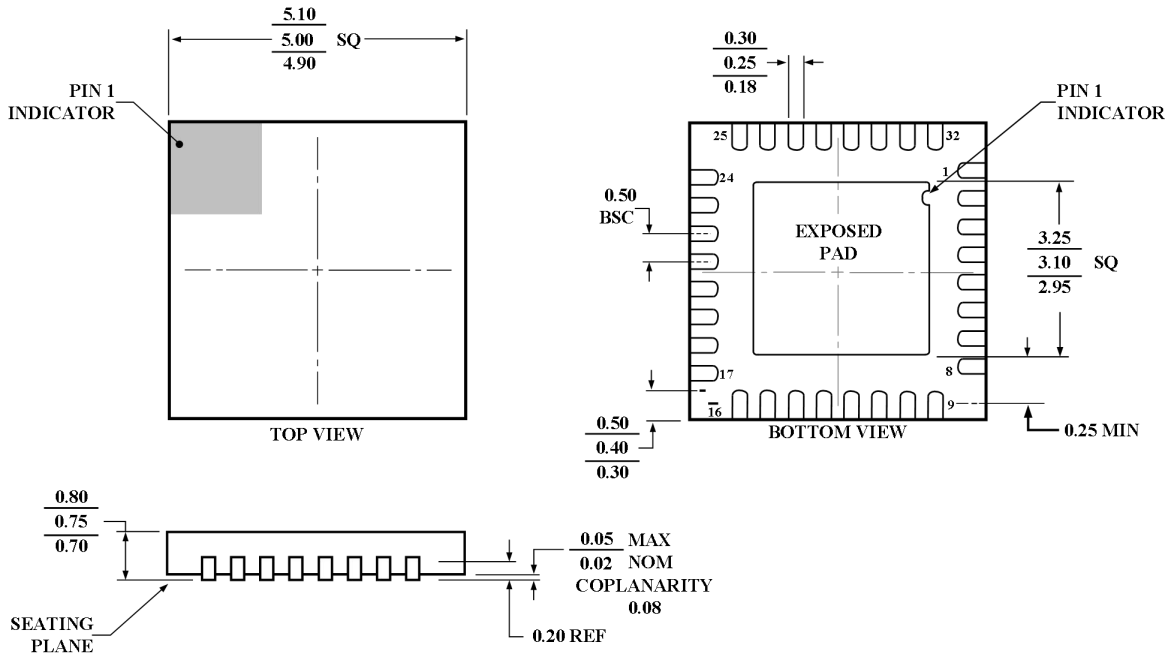


Figure 3 Package Outline Dimensions

Pin Configuration

Terminations of 18-bit A/D converter is shown in Figure 4

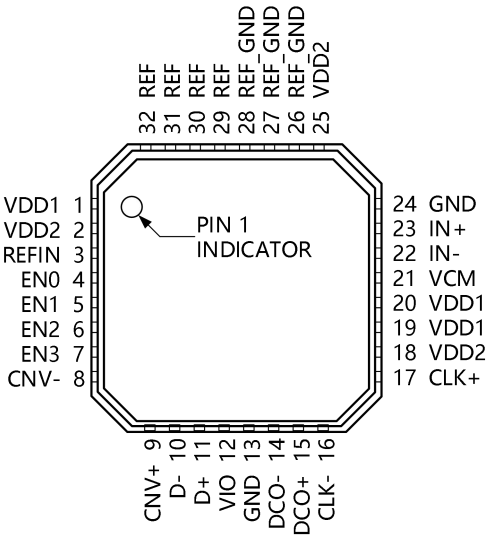


Figure 4 pin configuration

Pin Description

Pin Number	Symbol	Function	Pin Number	Symbol	Function
1	V_{DD1}	5V analog voltage	17	CLK+	clock input(+)
2	V_{DD2}	1.8 V analog voltage	18	V_{DD2}	1.8 V analog voltage
3	REF_{IN}	input end of reference voltage	19	V_{DD1}	5V analog voltage
4	EN_0	control terminal of operating state	20	V_{DD1}	5V analog voltage
5	EN_1	control terminal of operating state	21	VCM	common mode level output terminal
6	EN_2	control terminal of operating state	22	IN-	analog input terminal(-)
7	EN_3	control terminal of operating state	23	IN+	analog input terminal(+)
8	VNC-	conversion trigger input terminal (-)	24	GND	ground
9	VNC+	conversion trigger input terminal (+)	25	V_{DD2}	1.8 V analog voltage
10	D-	data Serial output terminal (-)	26	GND_{REF}	reference ground
11	D+	data Serial output terminal (+)	27	GND_{REF}	reference ground
12	V_{IO}	1.8 V port power supply	28	GND_{REF}	reference ground
13	GND	ground	29	V_{REF}	5V reference voltage
14	DCO-	clock output terminal (-)	30	V_{REF}	5V reference voltage
15	DCO+	clock output terminal (+)	31	V_{REF}	5V reference voltage
16	CLK-	clock output terminal (-)	32	V_{REF}	5V reference voltage
Note: heat sink connects analog source					

Recommended operation conditions

- analog supply voltage 1(VDD1): 4.75V ~ 5.25V
- analog supply voltage 2(VDD2): 1.71V ~ 1.89V
- I/O supply voltage(VIO): 1.71V ~ 1.89V
- range of analog common mode input voltage(VIC): 2.45V ~ 2.55V
- duty cycle of clock input: 50%±10%(TYP)
- clock input frequency of serial interface(fclk): 250MHz(TYP)
- Clock frequency(fs): 300MHz(MAX)
- operation ambient temperature(TA): -40℃ ~ 85℃
- Input range of analog signal: -5V ~ +5V
- operation input voltage: -0.1V ~ +5.1V
- Range of reference voltage: 4.096V~5V

Performance Index

parameter name	symbol	condition	performance index			Unit
			MIN	TYP	MAX	
resolution	*RES*	V_{DD1}=5V, V_{DD2}=1.8V, V_{IO}=1.8V,		18		Bits
electric current of VDD1	I_{VDD1}	EN0-EN3=1001, REFIN=0	—	0.9	2.0	mA
electric current of VDD2	I_{VDD2}	EN0-EN3=1001, REFIN=0	—	7.8	15	mA
electric current of VIO	I_{VIO}	EN0-EN3=1001, REFIN=0	—	9.0	15	mA
power dissipation	*PD*	EN0-EN3=1001, REFIN=0	—	35	75	mW
no missing codes *	—	f_{IN}=1kHz, V_{REF}=5V		18		Bits
Linear error	E_L	f_{IN}=1kHz, V_{REF}=5V	-6.0	+1.5/ -1.5	+6.0	LSB
differential error	E_{DL}	f_{IN}=1kHz, V_{REF}=5V	-0.99	+0.85/ -0.60	+1.75	LSB
transition noise	N_{TRA}	f_{IN}=DC, V_{REF}=5V	—	1.25	+5.0	LSB
offset error	E_O	f_{IN}=DC, V_{REF}=5V	-25	+1.00	+25	LSB
offset error drift	ΔE_O		-8	+0.20	+8	ppm/℃
gain error	E_G	f_{IN}=DC, V_{REF}=5V	-50	-10	+50	LSB

gain error drift	ΔE_G		-16	+0.20	+16	ppm/℃
digital input high level	V_{IH}	V_{DD1}=5V,V_{DD2}=1.8V,V_{IO}=1.8V	1.5	1.5	—	V
Digital input low level	V_{IL}		—	0.3	0.3	V
dynamic range	*DR*	f_{IN}=DC， V_{REF}=5V	94	97.5	—	dB
		f_{IN}=DC， V_{REF}=4.096V	93	96.0	—	
Signal-to-Noise Ratio	*SNR*	f_{IN}=1kHz， V_{REF}=5V	93	95.5	—	dB
		f_{IN}=1kHz， V_{REF}=4.096V	92	95.0	—	
effective bits	*ENOB*	f_{IN}=1kHz， V_{REF}=5V	14.9	15.70	—	bits
		f_{IN}=1kHz， V_{REF}=4.096V	14.8	15.60		bits
signal to noise distortion ratio	*SINAD*	f_{IN}=1kHz， V_{REF}=5V	92	95.0	—	dB
		f_{IN}=1kHz， V_{REF}=4.096V	91.5	94.5	—	dB
spurious-Free dynamic Range (SFDR)	*SFDR*	f_{IN}=1kHz， V_{REF}=5V	105	115.0	—	dB
		f_{IN}=1kHz， V_{REF}=4.096V	101	107.0	—	dB
total harmonic distortion	*THD*	f_{IN}=1kHz， V_{REF}=5V	—	-113.0	-101	dB
		f_{IN}=1kHz， V_{REF}=4.096V	—	-108.0	-98	dB
sample rate	S_{Rmax}	f_{IN}=1kHz， V_{REF}=5V	—	—	5	MSPS
conversion interval	t_{CYC}	f_{IN}=1kHz， V_{REF}=5V	200	200	—	ns
CNV high pulse resolution	t_{CNVH}	f_{IN}=1kHz， V_{REF}=5V	10	20	120	ns
output data sampling frequency	f_{CLK}	f_{IN}=1kHz， V_{REF}=5V	150	100	250	MHz
Delay of CLK to DCO	t_{DCO}	V_{DD1}=5V， V_{DD2}=1.8V， V_{IO}=1.8V，	0	2.8	10	ns
* No missing codes is characterized by differential error (E_{DL}) ,when E_{DL} > -1LSB it is considered to be no missing codes.						

Major Characteristic of Curves（test diagram of electric characteristic）

Test curve of DNL、INL:

Static state of 18-bit A/D converter is shown in Figure 5

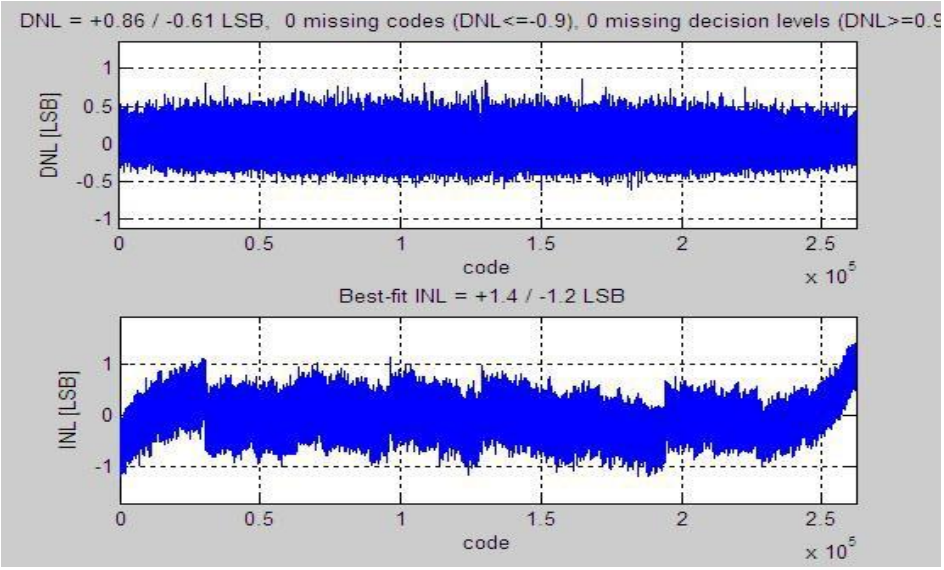
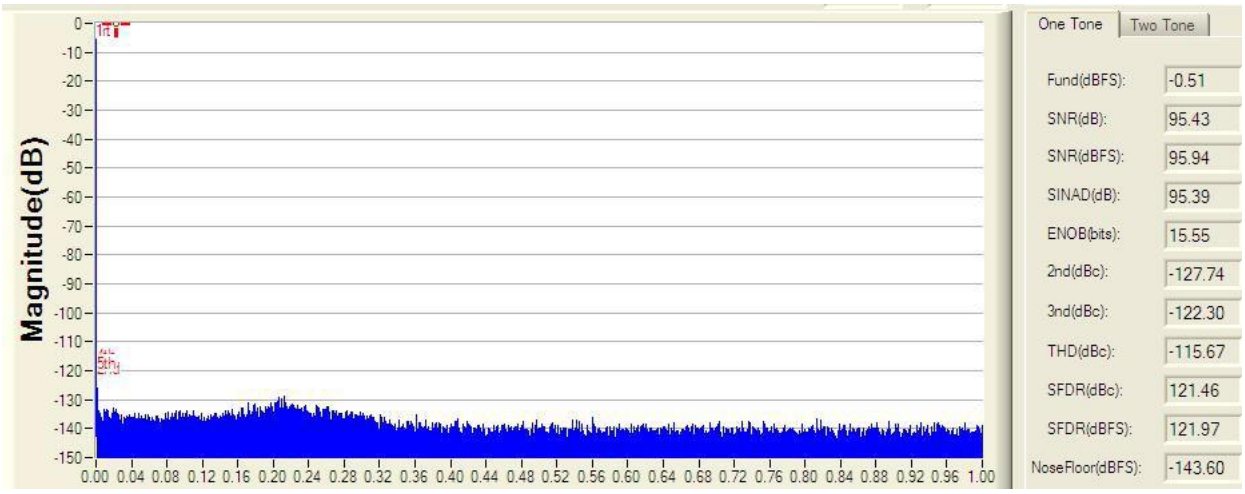


Figure 5. Static characteristic curves diagram of 18-bit A/D converter

Test curve of dynamic parameter:

FFT spectrum diagram 18-bit A/D converter is shown in Figure 6:

Test condition: sampling frequency: fCLK=5MHz, Input signal frequency: fIN=1kHz, Input signal amplitude: -1dBFS



Input signal frequency of 18-bit A/D converter VS dynamic performance

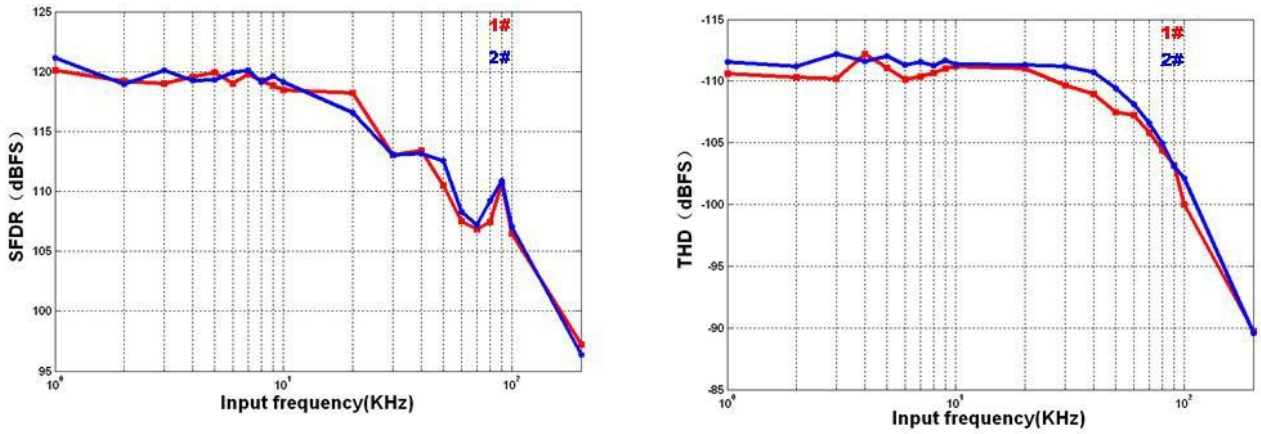
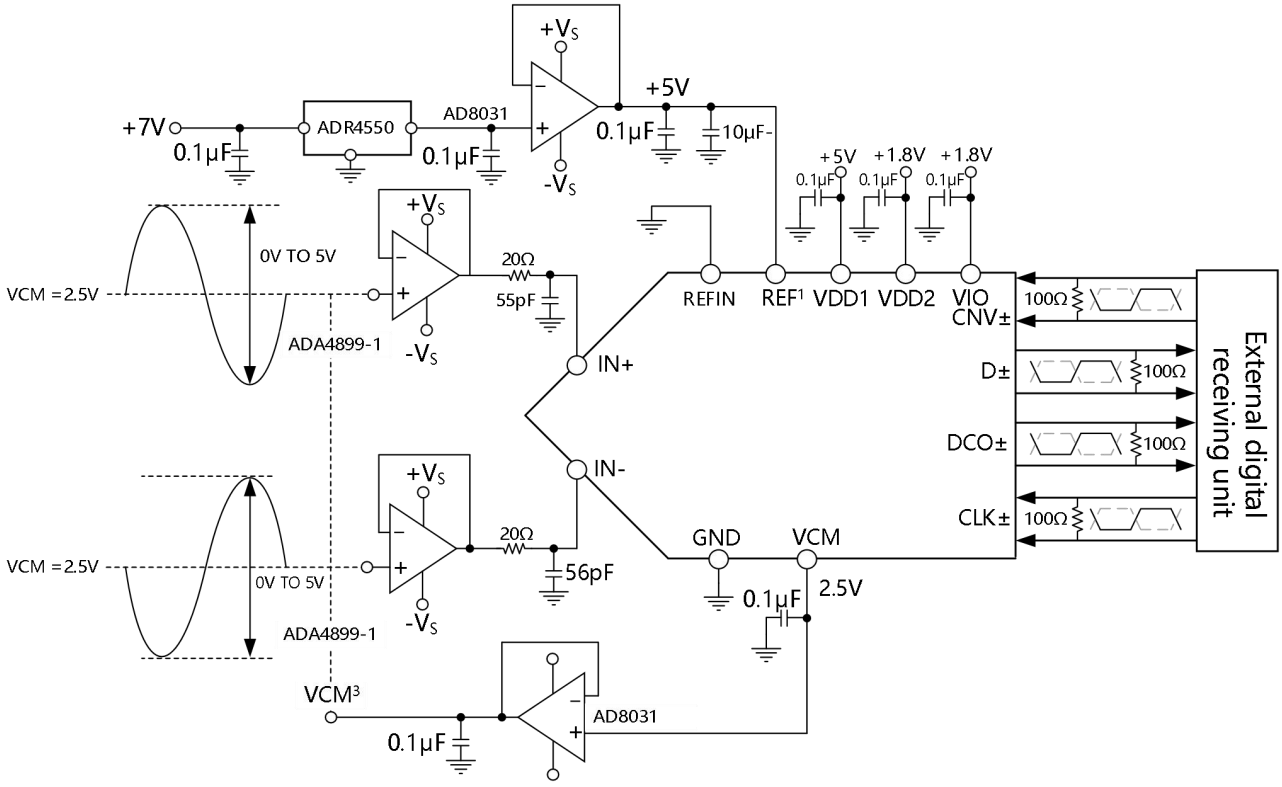


Figure 7 SFDR/SNR index of 18-bit A/D converter VS Input signal frequency

Typical application circuit diagram

The following figure is recommend application circuit diagram of A/D converter:



Matters Need Attention

1. installation:

When used, the circuit should avoid to be inserted reverse, it can lead to damage to circuit.

2. usage:

- The shipshape ground is required for the circuit board of application object.
- The application object should use multiring board including independence ground layer.
- The digital grounding and analog grounding of circuit board of application object should be separated as far as possible, digital line cannot arrange beside of analog line or under the ADC.
- AVDD, DRVDD and VCM should connect to ceramic bypass capacity of high quality and bypass capacity should approach pins, the line connecting pins to the bypass capacity is the shorter the better and the wider the better.
- Differential input should approach as much as possible and parallel each other.
- Input wires should be short as much as possible to minimize the input of parasitic capacitance and noise.
- It is important that the ground of chip should be connected to the PCB through as many channels as possible and plentiful area.

3. protection:

Although all the terminations of circuit are designed ESD protection structure, high energy electric pulse may be damaged the circuit. Electrostatic protection should be paid attention d during the test, transport and keep in reserve.

Common Failure Treatment method

1. zero output signal: Checking whether the Power supply voltage, Input Signal or clock are correct loading.
2. overflow signal occurs: Checking whether reference circuit is normal operation and whether amplitude of input signal is OK.
3. the device is unstable: Checking the power for guaranteeing stability of supply voltage

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PAKEAGE OPTION	MAKING INFORMATION
CBM79AD60G		-40℃-85℃	QFN-32	Tray，490	