Features

- **Dual transmitters**
- **Dual receivers**
- **Dual input observation receivers**
- **Minimum signal bandwidth 12kHz**
- **Maximum signal bandwidth 40MHz**
- **Integrated fractional-N frequency synthesizers**
- **Integrated clock synthesizer**
- **Multichip phase synchronization**
- **LVDS and CMOS synchronous serial data interface options**
- **Frequency range (center frequency) 10 MHz to 7250 MHz**
- **Each Rx/Tx can operate at different frequencies**
- **Fast frequency hopping**
- **Low power monitor and sleep modes**

Applications

- VHF, UHF and cellular communication
- TDD and FDD applications
- Phased array radar
- Test equipment

General Description

The CBMRF9002 is a highly integrated RF transceiver offering dual transmitters and dual receivers, integrated synthesizers, and digital signal processing functions.

The CBMRF9002 is a high performance, high linear, high dynamic range transceiver, and is extremely suitable for low power, portable and battery powered equipment.

The CBMRF9002 operates from 10MHz to 7250MHz. The device is capable of both TDD and FDD operation.

The CBMRF9002 consists of direct conversion signal paths with ideal noise figure and linearity. Each complete receiver and transmitter subsystem includes dc offset correction, quadrature error correction (QEC), and programmable digital filters, which eliminate the need for these functions in the digital baseband. In addition, several auxiliary functions, such as auxiliary analog-to-digital converters (ADCs), auxiliary digital-to-analog converters (DACs), and general-purpose inputs/outputs (GPIOs), are integrated to provide additional monitoring and control capability.

The fully integrated phase-locked loops (PLLs) provide high performance, low power, fractional-N frequency synthesis for the

transmitter, receiver, and clock sections. Careful design and layout techniques provide the isolation required in high performance personal radio applications.
All voltage controlled oscillator (VCO) and loop filter components are integrated to minimize the external component count. The local oscillators (LOs) have flexible configuration options and include fast lock modes.

The transceiver includes low power sleep and monitor modes to save power and extend the battery life of portable devices while monitoring communications.

CBMRF9002 supports multichip synchronization mechanism that synchronizes the phase of the RF local oscillator (LO) and digital clock.

The power supplies of CBMRF9002 include 1.0V, 1.3V and 1.8V. These voltages can be generated form linear regulators or switching regulators.

CBMRF9002 uses an SPI interface to communicate with the external processor.

High data rate and low data rate interfaces are supported using configurable CMOS or low voltage differential signaling (LVDS) serial synchronous interface (SSI) choice.

The CBMRF9002 is packaged in a 12 mm × 12 mm, 196-ball chip scale package ball grid array (CSP_BGA).

CBMRF9002BG supports an operating temperature range of -40~+85℃.

Datalog

Revision History

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.11.10					

Functional Block Diagram

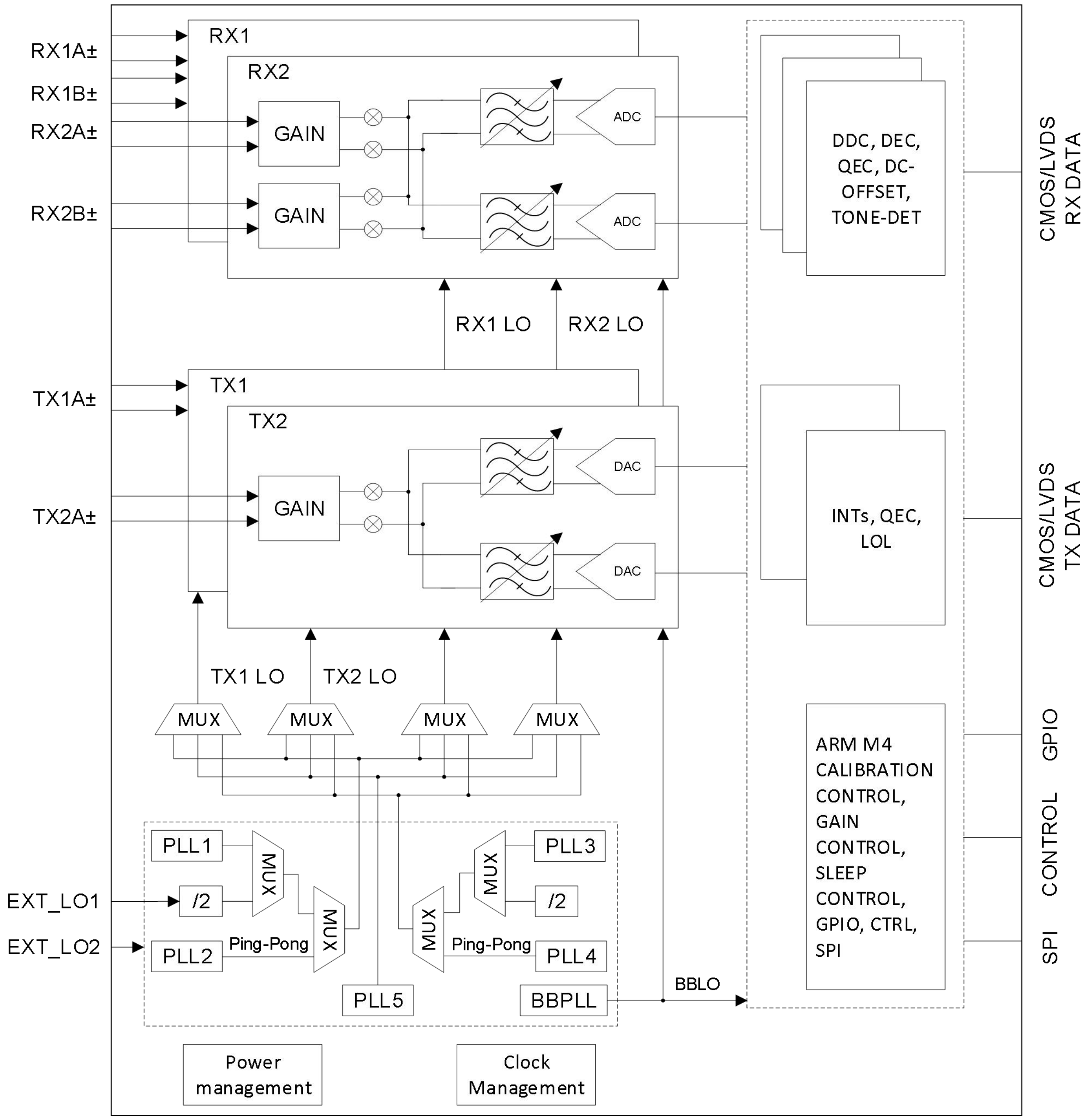

Figure 1 Functional Block Diagram

Specifications

Electrical characteristics at the operating ambient temperature range, VDDA_1P0 = 1.0 V, VDDA_1P3 = 1.3 V, VDDA_1P8 = 1.8 V, VDD_1P0 = 1.0 V, and VDD_1P8 = 1.8 V.

Operation configuration:

- RX BW 62.5MHz (IQ rate = 62.5MHz), analog gain = 0dB.
- TX BW 62.5MHz (IQ rate = 62.5MHz), analog attenuation, = 0dB.
- ORX BW 62.5MHz (IQ rate = 62.5MHz), analog attenuation, = 0dB.
- Reference clock = 125MHz.
- TX BW 62.5 MHz (IQ rate = 62.5 MHz), analog attenuation, = 0dB.
- RX channels represent RX1A or RX2A. ORX channels represent RX1B or RX2B.

Table 1

TRANSMITTERS

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Frequency range		10		7250	MHz	
Transmitter band width		0.012		100	MHz	
Transmitter pass band flatness			±1		dB	
Transmitter attenuation		0		34	dB	
Transmitter attenuation step			0.5		dB	
In Band Noise Floor						Test at LO+BW*0.25
			-148.4		dBm/Hz	LO=470MHz
			-147.5		dBm/Hz	LO=900MHz
			-144.1		dBm/Hz	LO=2400MHz
			-143.4		dBm/Hz	LO=3000MHz
Adjacent Channel Leakage Ratio	ACPR					100MHz bandwidth OFDM
			-57		dB	LO=0.7GHz, -13dBFs
			-55		dB	LO=2.595GHz, -12dBFs
			-53		dB	LO=4.88GHz, -15dBFs

Interpolation Images					dBc	
TX1 to TX2 Isolation			108.1		dB	LO=30MHz
			106.6		dB	LO=470MHz
			102.9		dB	LO=900MHz
			87.2		dB	LO=2400MHz
			87.2		dB	LO=3000MHz
Image Rejection Ratio	IRR					CW -6dBFS, Bandwidth 62.5MHz, 10MHz offset
			69		dBc	LO=30MHz
			62.8		dBc	LO=470MHz
			67.1		dBc	LO=900MHz
			67.7		dBc	LO=2400MHz
			73.9		dBc	LO=3000MHz
Maximum Output Power						Digital power -0.2dBFs
			6.98		dBm	LO=30MHz
			7.38		dBm	LO=470MHz
			6.72		dBm	LO=900MHz
			5.68		dBm	LO=2400MHz
					dBm	LO=3000MHz
Third-Order Output intermodulation intercept Point	OIP3					0 dB transmitter attenuation, CW -11dBFS
			28.5		dBm	LO=30MHz
			29.1		dBm	LO=470MHz
			29.3		dBm	LO=900MHz
			29.2		dBm	LO=2400MHz
			23.6		dBm	LO=3000MHz
Carrier Leakage	LOL					CW -6dBFS
			-65.7		dBm	LO=30MHz
			-62.7		dBm	LO=470MHz
			-65.1		dBm	LO=900MHz
			-68.3		dBm	LO=2400MHz

			-70.1		dBm	LO=3000MHz
Error Vector Magnitude	EVM					3GPP TM3.1A test signal
					%	LO=2.595GHz
Output impedance	Z_{OUT}		50		Ω	Differential

Table 2

RECEIVERS

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Frequency range		10		7250	MHz	
Gain Range		0		34	dB	
Analog Gain Step			0.5		dB	
Bandwidth Ripple			±1		dB	Without bandwidth ripple calibration
Receiver Bandwidth		0.012		100	MHz	
Maximum Input Signal Power	P_{HIGH}					CW 0dB attenuation, received digital power -0.5/-1dBFS
			-11.7		dBm	LO=30MHz
			-11.8		dBm	LO=470MHz
			-12.0		dBm	LO=900MHz
			-10.3		dBm	LO=2400MHz
			-9.4		dBm	LO=3000MHz
Third-Order Input Intermodulation Intercept Point	IIP3					Two tone signal, LO+17MHz/18MHz
			11.07		dBm	LO=30MHz
			11.94		dBm	LO=470MHz
			13.63		dBm	LO=900MHz
			13.50		dBm	LO=2400MHz
			14.11		dBm	LO=3000MHz
Third-Order Harmonic Distortion Product	HD3					Received signal -18dBm, offset 5MHz

			-63.1		dBc	LO=30MHz
			-69.1		dBc	LO=470MHz
			-72.1		dBc	LO=900MHz
			-76.7		dBc	LO=2400MHz
			-74.9		dBc	LO=3000MHz
Second-Order Intermodulation Distortion	IM2					Two tone signal, LO+17MHz/18MHz
			-73.8		dBc	LO=30MHz
			-65.4		dBc	LO=470MHz
			-71.9		dBc	LO=900MHz
			-69.5		dBc	LO=2400MHz
			-68.1		dBc	LO=3000MHz
Image Rejection			-75.1		dBc	LO=30MHz
			-66.5		dBc	LO=470MHz
			-75.3		dBc	LO=900MHz
			-69.1		dBc	LO=2400MHz
			-60.1		dBc	LO=3000MHz
Input Impedance					Ω	Differential
RX1 to RX2 Isolation			100		dB	LO=30MHz
			100		dB	LO=470MHz
			100		dB	LO=900MHz
			100		dB	LO=2400MHz
			100		dB	LO=3000MHz
Receiver Band Spurs						-5dBFs receiver signal
			-65.8		dBc	LO=30MHz
			-63.4		dBc	LO=470MHz
			-63.2		dBc	LO=900MHz
			-62.9		dBc	LO=2400MHz
			-60.6		dBc	LO=3000MHz
Receiver DC offset			-75.4		dBFs	LO=30MHz
			-74.7		dBFs	LO=470MHz
			-73.7		dBFs	LO=900MHz

			-68.3		dBFs	LO=2400MHz
			-71.1		dBFs	LO=3000MHz

Table 3

LOCAL OSCILLATOR

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Phase Noise 470MHz			-96.9		dBc/Hz	100Hz offset
			-106.4		dBc/Hz	1kHz offset
			-113.3		dBc/Hz	10kHz offset
			-116.8		dBc/Hz	100kHz offset
			-134.9		dBc/Hz	1MHz offset
			-145.7		dBc/Hz	10MHz offset
Phase Noise 900MHz			-91.5		dBc/Hz	100Hz offset
			-100.9		dBc/Hz	1kHz offset
			-10.78		dBc/Hz	10kHz offset
			-111.2		dBc/Hz	100kHz offset
			-132.4		dBc/Hz	1MHz offset
			-148.6		dBc/Hz	10MHz offset
Phase Noise 2400MHz			-84.2		dBc/Hz	100Hz offset
			-92.2		dBc/Hz	1kHz offset
			-99.6		dBc/Hz	10kHz offset
			-102.8		dBc/Hz	100kHz offset
			-129.1		dBc/Hz	1MHz offset
			-147.7		dBc/Hz	10MHz offset
Phase Noise 3500MHz			-78.2		dBc/Hz	100Hz offset
			-92.1		dBc/Hz	1kHz offset
			-100.5		dBc/Hz	10kHz offset
			-102.7		dBc/Hz	100kHz offset
			-126.8		dBc/Hz	1MHz offset
			-146.7		dBc/Hz	10MHz offset
LO Phase Synchronization					Degrees	

Lock Time					ms	
Fast Lock Time					us	
Frequency Hopping					hop/s	

Table 4

REFCLK

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Type			LVDS			
Input Frequency		50		1000	MHz	
Signal Level		0.2		0.8	Vpp	
Common-mode Voltage			1.2		V	
Input Differential Impedance			100		Ω	External resistor needed
Clock output frequency		10		7250	MHz	

Table 5

POWER SUPPLY

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
VOLTAGE CHARACTERISTICS						
VDDA1P0 Voltage		0.98	1.0	1.03	V	
VDDD1P0 Voltage		0.90	1.0	1.1	V	
VDDA1P3 Voltage		1.25	1.3	1.35	V	
VDDA1P8 Voltage		1.70	1.8	1.90	V	
VDDD1P8 Voltage		1.62	1.8	1.98	V	
SUPPLY CURRENT						
VDDA1P0 Voltage					A	
VDDD1P0 Voltage					A	
VDDA1P3 Voltage					A	
VDDA1P8 Voltage					A	
VDDD1P8 Voltage					A	

Total Power Dissipation					W	

Absolute Maximum Ratings

Table 6

Parameter	Range
VDDA1P0 to VSSA	-0.2V to +1.2V
VDDA1P3 to VSSA	-0.2V to +1.5V
VDDA1P8 to VSSA	-0.3V to +2.0V
VDDD1P0 to VSSD	-0.2V to +1.2V
VDDD1P8 to VSSA	-0.3V to +2.2V
Maximum T_J	125℃
Storage Temperature Range	-65℃ to +150℃
Operating Temperature Range	-40~+85℃

Thermal Management

The CBMRF9002 uses an exposed die package to provide the customer with the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly. Figure 2 shows a typical thermal management solution.

To avoid damage, an over-temperature protect mechanism is integrated. When the junction temperature rises over 130 ℃, the transmitters and receivers will be shut down, and the over-temperature status can be read out.

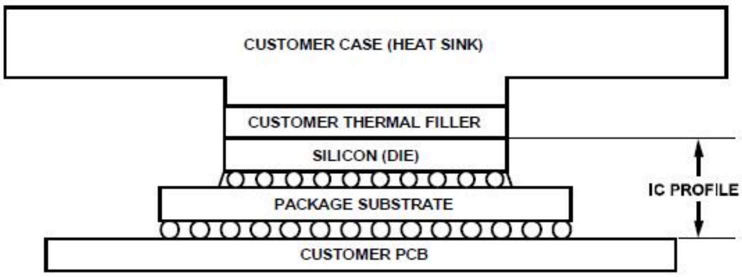

Figure 2 Typical Thermal Management Solution

Thermal Resistance		
Parameter	Type	**Unit**
Rjs	2	K/W
Rjs-top	0.03	K/W

Pin Configuration and Function Descriptions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	VSSA	EXT_LO2+	EXT_LO2-	VRFVCO2_1P3	VRFLO2_1P0	MODEA	RBIAS	VRFLO1_1P0	VRFVCO1_1P3	EXT_LO1-	EXT_LO1+	VSSA	VSSA
B	RX2A-	VSSA	VSSA	VSSA	VSSA	VRFVCO2_1P0	AUXADC_2	AUXADC_1	VRFVCO1_1P0	VSSA	VSSA	VSSA	VSSA	RX1A-
C	RX2A+	VSSA	RX2B+	RX2B-	VSSA	VANA2_1P0	VANA2_1P3	VANA1_1P3	VANA1_1P0	VSSA	RX1B-	RX1B+	VSSA	RX1A+
D	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	MCS+	MCS-	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
E	VRX2LO_1P0	VRX2LO_1P3	AGPIO_2	VRFSYN2_1P3	VCLKSYN_1P3	VSSA	DEV_CLK_IN+	DEV_CLK_IN-	VSSA	VAUXSYN_1P3	VRFSYN1_1P3	AGPIO_0	VRX1LO_1P3	VRX1LO_1P0
F	VSSA	VSSA	VSSA	AGPIO_4	AGPIO_3	VSSA	VSSA	VSSA	VSSA	AGPIO_1	AGPIO_10	VSSA	VSSA	VSSA
G	TX2+	VSSA	VTX2LO_1P3	AGPIO_5	VCLKVCO_1P3	AGPIO_6	VCONV_1P8	VAGPIO_1P8	AGPIO_8	VAUXVCO_1P3	AGPIO_11	VTX1LO_1P3	VSSA	TX1+
H	TX2-	VANA2_1P8	VTX2LO_1P0	AUXADC_3	VCLKVCO_1P0	AGPIO_7	VCONV_1P0	VCONV_1P3	AGPIO_9	VAUXVCO_1P0	AUXADC_0	VTX1LO_1P0	VANA1_1P8	TX1-
J	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
K	SPI_CLK	SPI_DIO	RX2_EN	VSSA/TESTCK+	VSSA/TESTCK-	DGPIO_0	DGPIO_1	DGPIO_2	DGPIO_3	DGPIO_4	DGPIO_5	RX1_EN	RESETB	GP_INT
L	SPI_EN	SPI_DO	TX2_EN	DGPIO_6	DGPIO_7	DGPIO_8	VDIG_1P0	VDIG_1P0	DGPIO_9	DGPIO_10	DGPIO_11	TX1_EN	MODE	DEV_CLK_OUT
M	RX2_IDATA_OUT-	RX2_IDATA_OUT+	RX2_DCLK_OUT-	RX2_DCLK_OUT+	DGPIO_15/TX2_DCLK_OUT+	DGPIO_14/TX2_DCLK_OUT-	VDIGIO_1P8	VDIG_0P9	DGPIO_12/TX1_DCLK_OUT-	DGPIO_13/TX1_DCLK_OUT+	RX1_DCLK_OUT+	RX1_DCLK_OUT-	RX1_IDATA_OUT+	RX1_IDATA_OUT-
N	RX2_STROBE_OUT-	RX2_STROBE_OUT+	RX2_QDATA_OUT-	RX2_QDATA_OUT+	TX2_DCLK_IN+	TX2_DCLK_IN-	VSSD	VSSD	TX1_DCLK_IN-	TX1_DCLK_IN+	RX1_QDATA_OUT+	RX1_QDATA_OUT-	RX1_STROBE_OUT+	RX1_STROBE_OUT-
P	VSSD	TX2_STROBE_IN+	TX2_STROBE_IN-	TX2_QDATA_IN-	TX2_QDATA_IN+	TX2_IDATA_IN+	TX2_IDATA_IN-	TX1_IDATA_IN-	TX1_IDATA_IN+	TX1_QDATA_IN+	TX1_QDATA_IN-	TX1_STROBE_IN-	TX1_STROBE_IN+	VSSD

Figure 3 Pin Configuration (Top View)

Table 10 Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Type	Mnemonic	Description
A1, A2, A13, A14, B2 to B5, B10 to B13, C2, C5, C10, C13, D1 to D6, D9 to D14, E6, E9, F1 to F3, F6 to F9, F12 to F14, G2, G13, J1 to J14	Input	VSSA	Analog Ground.
A3, A4	Input / Output	EXT_LO2+, EXT_LO2-	Input: External LO input, the input frequency must be 2 times the LO. Output: output the LO.
A5	Input	VRFVCO2_1P3	1.3 V Internal LDO Regulator Input Supply for RF External LO Input 2 (LO2) VCO and LO Generation Circuitry.
A6	Input / Output	VRFLO2_1P0	1.0 V Internal Supply Node for RF LO2 LO Generation Circuitry. Connect VRFLO2_1P0 together with VRFVCO2_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO2_1P3 input is in use. Provide a 1.0 V supply to VRFLO2_1P0 when the internal LDO regulator that is operated from VRFVCO2_1P3 is not in use.
A7	Input	MODEA	Mode Configuration.
A8	Input	RBIAS	Bias Resistor Connection. RBIAS generates an internal current based on an external 1% resistor. Connect a 4.99 kΩ resistor between RBIAS and VSSA (analog ground).
A9	Input / Output	VRFLO1_1P0	1.0 V Internal Supply Node for RF LO1 LO Generation Circuitry. Connect VRFLO1_1P0 together with VRFVCO1_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO1_1P3 input is in use. Provide a 1.0 V supply to VRFLO1_1P0 when the internal LDO regulator operated from VRFVCO1_1P3 is not in use.
A10	Input	VRFVCO1_1P3	1.3 V Internal LDO Input Supply for RF LO1 VCO and LO

			Generation Circuitry. VRFVCO1_1P3 is sensitive to supply noise.
A11, A12	Input	EXT_LO1-, EXT_LO1+	Differential External LO Input 2. If EXT_LO1+ and EXT_LO1− are used for the external LO2, the input frequency must be 2× or higher than the desired carrier frequency. For an LO range from 500 MHz to 1 GHz, a 1 × multiplier is available. If unused, connect EXT_LO1+ and EXT_LO1− to VSSA.
B1, C1	Input	RX2A-, RX2A+	Differential Input A for Rx2. If unused, connect RX2A− and RX2A+ to VSSA.
B6	Output	VRFVCO2_1P0	1.0 V Internal Supply Node for RF LO2 VCO Circuitry. Connect this VRFVCO2_1P0 together with VRFLO2_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO2_1P3 input is in use.
B7	Input	AUXADC_2	Input 2 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_2.
B8	Input	AUXADC_1	Input 1 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_1.
B9	Output	VRFVCO1_1P0	1.0 V Internal Supply node for RF LO1 VCO Circuitry. Connect VRFVCO1_1P0 together with VRFLO1_1P0 and bypass with a 4.7 μF capacitor when the internal LDO regulator operated from the VRFVCO1_1P3 input is in use.
B14, C14	Input	RX1A-, RX1A+	Differential Input A for Rx1. If unused, connect RX1A− and RX1A+ to VSSA.
C3, C4	Input	RX2B+, RX2B-	Differential Input B for Rx2. If unused, connect RX2B+ and RX2B− to VSSA.
C6	Input / Output	VANA2_1P0	1.0 V Internal Supply Node for Tx2 and Rx2 Baseband Circuits, TIA, Transmitter Transconductance (GM) Baseband Filters, and Auxiliary DACs and ADCs. For normal operation, leave VANA2_1P0 unconnected.
C7	Input	VANA2_1P3	1.3 V Internal LDO Input Supply for Tx2 and Rx2 Baseband Circuits, TIA, Transmitter GM, Baseband Filters, and Auxiliary DACs and ADCs. VANA2_1P3 is sensitive to supply noise.
C8	Input	VANA1_1P3	1.3 V Internal LDO Input Supply for Tx1 and Rx1 Baseband Circuits, TIA, Transmitter GM and Baseband Filters. VANA1_1P3 is sensitive to supply noise.
C9	Input / Output	VANA1_1P0	1.0 V Internal Supply Node for Tx1 and Rx1 Baseband Circuits, TIA, Transmitter GM and Baseband Filters. For normal operation, leave VANA1_1P0 unconnected.
C11, C12	Input	RX1B-,RX1B+	Differential Input B for Rx1. If unused, connect RX1B− and RX1B+ to VSSA.
D7, D8	Input	MCS+, MCS-	Multichip Synchronization Reference Inputs. If unused, connect MCS+ and MCS− to VSSA.
E1	Output	VRX2LO_1P0	1.0 V Internal Supply Node for Rx2 LO Buffers and Mixers. VRX2LO_1P0 is sensitive to supply noise. Bypass VRX2LO_1P0 with a 4.7 μF capacitor.
E2	Input	VRX2LO_1P3	1.3 V Internal LDO Input Supply for Rx2 LO Buffers and Mixers. Provide a 1.0 V supply to VRX2LO_1P3 when the internal LDO regulator is not used. VRX2LO_1P3 is sensitive to supply noise.

E3, E12, F4, F5, F10, F11, G4, G6, G9, G11, H6, H9	Input / Output	AGPIO_xx	GPIOs Signals Referenced to VAGPIO_1P8 1.8 V Supply.
E4	Input		1.3 V Supply for RF LO2 Synthesizer. VRFSYN2_1P3 is sensitive to supply noise.
E5	Input		1.3 V Supply for Clock Synthesizer. VCLKSYN_1P3 is sensitive to supply noise.
E7, E8	Input		Device Clock Input. DEV_CLK_IN± can operate as differential, single-ended, or be connected to the external crystal oscillator. In single-ended mode, apply the clock signal to the DEV_CLK_IN+ pin and leave the DEV_CLK_IN− pin unconnected.
E10	Input	VAUXSYN_1P3	1.3 V Supply for Auxiliary Synthesizer. VAUXSYN_1P3 is sensitive to supply noise.
E11	Input	VRFSYN1_1P3	VRFSYN1_1P3 1.3 V Supply for RF LO1 Synthesizer. VRFSYN1_1P3 is sensitive to supply noise.
E13	Input	VRX1LO_1P3	1.3 V Internal LDO Input Supply for Rx1 LO Buffers and Mixers. Provide a 1.0 V supply to VRX1LO_1P3 when the internal LDO regulator is not used. VRX1LO_1P3 is sensitive to supply noise.
E14	Output	VRX1LO_1P0	1.0 V Internal Supply Node for Rx1 LO Buffers and Mixers. VRX1LO_1P0 is sensitive to supply noise. Bypass VRX1LO_1P0 with a 4.7 μF capacitor.
G1, H1	Output	TX2+, TX2−	Differential Output for Transmitter Channel 2. If unused, do not connect TX2+ and TX2−.
G3	Input	VTX2LO_1P3	1.3 V Supply for Tx2 LO Buffers, Upconverter, and LO Delay. Provide a 1.0 V supply to VTX2LO_1P3 when the internal LDO is not used. VTX2LO_1P3 is sensitive to supply noise.
G5	Input	VCLKVCO_1P3	1.3 V Internal LDO Input Supply for Clock LO VCO and LO Generation Circuitry. VCLKVCO_1P3 is sensitive to supply noise.
G7	Input	VCONV_1P8	1.8 V Supply for Tx1 and Tx2 DAC and Rx1 and Rx2 ADC.
G8	Input	VAGPIO_1P8	1.8 V Supply for Auxiliary DACs, Auxiliary ADCs, and AGPIO Signals.
G10	Input	VAUXVCO_1P3	1.3 V Internal LDO Input Supply for Auxiliary LO VCO and LO Generation Circuitry. VAUXVCO_1P3 is sensitive to supply noise.
G12	Input	VTX1LO_1P3	1.3 V Internal LDO Input Supply for Tx1 LO Buffers, Upconverter, and LO Delay. Provide a 1.0 V supply to VTX1LO_1P3 when the internal LDO regulator is not used. VTX1LO_1P3 is sensitive to supply noise.

G14, H14	Output	TX1+, TX1−	Differential Output for Transmitter Channel 1. If unused, do not connect TX1+ and TX1−.
H2	Input	VANA2_1P8	1.8 V Supply for Rx2 Mixer, Rx2 TIA, Tx2 LPF, and Internal References.
H3	Output	VTX2LO_1P0	1.0 V Internal Supply Node for Tx2 LO Buffers, Upconverter, and LO Delay. For normal operation, leave VTX2LO_1P0 unconnected.
H4	Input	AUXADC_3	Input 3 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_3.
H5	Output	VCLKVCO_1P0	1.0 V Internal Supply Node for Clock LO VCO and LO Generation Circuitry. Bypass VCLKVCO_1P0 with a 4.7 μF capacitor.
H7	Output	VCONV_1P0	1.0 V Internal Supply Node for Receiver ADCs and Transmitter DACs. Bypass VCONV_1P0 with a 4.7 μF capacitor.
H8	Input	VCONV_1P3	1.3 V Internal LDO Input Supply for Receiver ADCs and Transmitter DACs. Provide a 1.0 V supply to VCONV_1P3 when the internal LDO regulator is not used. VCONV_1P3 is sensitive to supply noise.
H10	Output	VAUXVCO_1P0	1.0 V Internal Supply Node for Auxiliary LO VCO and LO Generation Circuitry. Bypass VAUXVCO_1P0 with a 4.7 μF Capacitor.
H11	Input	AUXADC_0	Input 0 to Auxiliary ADC Input Multiplexer. If unused, do not connect AUXADC_0.
H12	Output	VTX1LO_1P0	1.0 V Internal Supply Node for Tx1 LO Buffers, Upconverter, and LO Delay. For normal operation, leave VTX1LO_1P0 unconnected.
H13	Input	VANA1_1P8	1.8 V Supply for Rx1 Mixer, Rx1 TIA, Tx1 LPF, Crystal Oscillator, DEV_CLK Circuitry, and Internal References.
K1	Input	SPI_CLK	Serial Data Bus Clock Input.
K2	Input / Output	SPI_DIO	Serial Data Input in 4-Wire Mode or Input and Output in 3-Wire Mode.
K3	Input	RX2_EN	Enable Input for Rx2. If unused, do not connect RX2_EN.
K4	Input	VSSA/TESTCK+	Connect VSSA/TESTCK+ to VSSA for normal operation.
K5	Input	VSSA/TESTCK-	Connect VSSA/TESTCK− to VSSA for normal operation.
K6 to K11, L4 to L6, L9 to L11	Input / Output	DGPIO_xx	Digital GPIO. VDIGIO_1P8 supplies 1.8 V to DGPIO_xx.
K12	Input	RX1_EN	Enable Input for Rx1. If unused, do not connect RX1_EN.
K13	Input	RESETB	Active Low Chip Reset.
K14	Output	GP_INT	General-Purpose Digital Interrupt Output Signal. If unused, do not connect GP_INT.
L1	Input	SPI_EN	Active Low Serial Data Bus Chip Select.

L2	Output	SPI_DO	Serial Data Output. If unused in SPI 3-wire mode, do not connect SPI_DO.
L3	Input	TX2_EN	Enable Input for Transmitter Channel 2. If unused, do not connect TX2_EN.
L7, L8	Input	VDIG_1P0	1.0 V Digital Core. Connect Pin L7 and Pin L8 together. Use a wide trace to connect the VDIG_1P0 pins to a separate power supply domain. Provide reservoir capacitance close to the chip.
L12	Input	TX1_EN	Enable Input for Transmitter Channel 1. If unused, do not connect TX1_EN.
L13	Input	MODE	Joint Test Action Group (JTAG) Boundary Scan Pin.
L14	Output	DEV_CLK_OUT	Single-Ended Device Clock Output. DEV_CLK_OUT provides a DEV_CLK signal or the divided version to the baseband IC. If unused, do not connect DEV_CLK_OUT.
M1	Output	RX2_IDATA_OUT−	In LVDS SSI mode, RX2_IDATA_OUT− is the Rx2 I sample data output on the negative side or the Rx2 I and Q sample data output on the negative side. In CMOS SSI mode, RX2_IDATA_OUT− is the Rx2 Data Output 0 or the Rx2 I and Q sample data output. If unused, do not connect RX2_IDATA_OUT−.
M2	Output	RX2_IDATA_OUT+	In LVDS SSI mode, RX2_IDATA_OUT+ is the Rx2 I sample data output positive side of the differential pair or the Rx2 I and Q sample data output positive side of the differential pair. In CMOS SSI mode, RX2_IDATA_OUT+ is the Rx2 Data Output 1. If unused, do not connect RX2_IDATA_OUT+.
M3	Output	RX2_DCLK_OUT−	In LVDS SSI mode, RX2_DCLK_OUT− is the Rx2 data clock output negative side. In CMOS SSI mode, RX2_DCLK_OUT− is not used. If unused, do not connect RX2_DCLK_OUT−.
M4	Output	RX2_DCLK_OUT+	In LVDS SSI mode, RX2_DCLK_OUT+ is the Rx2 data clock output positive side. In CMOS SSI mode, RX2_DCLK_OUT+ is the Rx2 data clock output. If unused, do not connect RX2_DCLK_OUT+.
M5	Input / Output	DGPIO_15/TX2_DCLK_OUT+	Digital GPIO 15. VDIGIO_1P8 supplies 1.8 V to DGPIO_15/TX2_DCLK_OUT+. Alternative function of DGPIO_15/TX2_DCLK_OUT+ is to provide the positive side of the reference clock output for the Tx2 data port in LVDS SSI mode. If unused, do not connect DGPIO_15/TX2_DCLK_OUT+.
M6	Input / Output	DGPIO_14/TX2_DCLK_OUT−	Digital GPIO 14. VDIGIO_1P8 supplies 1.8 V to DGPIO_14/TX2_DCLK_OUT−. The alternative function of DGPIO_14/TX2_DCLK_OUT− is to provide the negative side of the reference clock output for the Tx2 data port in LVDS SSI mode. If unused, do not connect DGPIO_14/TX2_DCLK_OUT−.
M7	Input	VDIGIO_1P8	1.8 V Supply Input for Data Port Interface (CMOS-SSI and LVDS SSI Mode), SPI Signals, Control Input and Output Signals, and DGPIO Interface.

M8	Output	VDIG_0P9	1.0 V Internal Supply Node for Digital Circuitry. Bypass VDIG_0P9 with a 4.7 μF capacitor.
M9	Input / Output	DGPIO_12/TX1_DCLK_OUT−	Digital GPIO 12. VDIGIO_1P8 supplies 1.8 V to DGPIO_12/TX1_DCLK_OUT−. The alternative function of DGPIO_12/TX1_DCLK_OUT− is to provide the negative side of the reference clock output for the Tx1 data port in LVDS SSI mode. If unused, do not connect DGPIO_12/TX1_DCLK_OUT−.
M10	Input / Output	DGPIO_13/TX1_DCLK_OUT+	Digital GPIO 13. VDIGIO_1P8 supplies 1.8 V to DGPIO_13/TX1_DCLK_OUT+. The alternative function of DGPIO_13/TX1_DCLK_OUT+ is to provide the positive side of the reference clock output for the Tx1 data port in LVDS SSI mode. If unused, do not connect DGPIO_13/TX1_DCLK_OUT+.
M11	Output	RX1_DCLK_OUT+	In LVDS SSI mode, RX1_DCLK_OUT+ is the Rx1 data clock output positive side. In CMOS SSI mode, RX1_DCLK_OUT+ is the Rx1 data clock output. If unused, do not connect RX1_DCLK_OUT+.
M12	Output	RX1_DCLK_OUT−	In LVDS SSI mode, RX1_DCLK_OUT− is the Rx1 data clock output negative side. In CMOS SSI mode, RX1_DCLK_OUT− is not used. If unused, do not connect RX1_DCLK_OUT−.
M13	Output	RX1_IDATA_OUT+	In LVDS SSI mode, RX1_IDATA_OUT+ is the Rx1 I sample data output positive side or the Rx1 I and Q sample data output positive side. In CMOS SSI mode, RX1_IDATA_OUT+ is the Rx1 Data Output 1.
M14	Output	RX1_IDATA_OUT−	In LVDS SSI mode, RX1_IDATA_OUT− is the Rx1 I sample data output negative side or the Rx1 I and Q sample data output negative side. In CMOS SSI mode, RX1_IDATA_OUT− is the Rx1 Data Output 0 or the Rx1 I and Q sample data output.
N1	Output	RX2_STROBE_OUT−	In LVDS SSI mode, RX2_STROBE_OUT− is the Rx2 strobe output negative side. In CMOS SSI mode, RX2_STROBE_OUT− is not used. If unused, do not connect RX2_STROBE_OUT−.
N2	Output	RX2_STROBE_OUT+	In LVDS SSI mode, RX2_STROBE_OUT+ is the Rx2 strobe output positive side. In CMOS SSI mode, RX2_STROBE_OUT+ is the Rx2 strobe output. If unused, do not connect RX2_STROBE_OUT+.
N3	Output	RX2_QDATA_OUT−	In LVDS SSI mode, RX2_QDATA_OUT− is the Rx2 Q sample data output positive side. In CMOS SSI mode, RX2_QDATA_OUT− is the Rx2 Data Output 2. If unused, do not connect RX2_QDATA_OUT−.
N4	Output	RX2_QDATA_OUT+	In LVDS SSI mode, RX2_QDATA_OUT+ is the Rx2 Q sample data output positive side. In CMOS SSI mode, RX2_QDATA_OUT+ is the Rx2 Data Output 3. If unused, do not connect RX2_QDATA_OUT+.
N5	Input	TX2_DCLK_IN+	In LVDS SSI mode, TX2_DCLK_IN+ is the Tx2 data clock input positive side. In CMOS SSI mode, TX2_DCLK_IN+ is the Tx2 data clock input. If unused, do not connect TX2_DCLK_IN+.

N6	Input	TX2_DCLK_IN-	In LVDS SSI mode, TX2_DCLK_IN− is the Tx2 data clock input negative side. In CMOS SSI mode, TX2_DCLK_IN− is not used. If unused, do not connect TX2_DCLK_IN−.
N7, N8, P1, P14	Input / Output	VSSD	Digital Supply Voltage (VSSD).
N9	Input	TX1_DCLK_IN−	In LVDS SSI mode, TX1_DCLK_IN− is the Tx1 data clock input negative side. In CMOS SSI mode, TX1_DCLK_IN− is not used. If unused, do not connect TX1_DCLK_IN−.
N10	Input	TX1_DCLK_IN+	In LVDS SSI mode, TX1_DCLK_IN+ is the Tx1 data clock input positive side. In CMOS SSI mode, TX1_DCLK_IN+ is the Tx1data clock input. If unused, do not connect TX1_DCLK_IN+.
N11	Output	RX1_QDATA_OUT+	In LVDS SSI mode, RX1_QDATA_OUT+ is the Rx1 Q sample data output positive side. In CMOS SSI mode, RX1_QDATA_OUT+ is the Rx1 Data Output 3. If unused, do not connect RX1_QDATA_OUT+.
N12	Output	RX1_QDATA_OUT−	In LVDS SSI mode, RX1_QDATA_OUT− is the Rx1 Q sample data output positive side. In CMOS SSI mode, RX1_QDATA_OUT− is the Rx1 Data Output 2. If unused, do not connect RX1_QDATA_OUT−.
N13	Output	RX1_STROBE_OUT+	In LVDS SSI mode, RX1_STROBE_OUT+ is the Rx1 strobe output positive side. In CMOS SSI mode, RX1_STROBE_OUT+ is the Rx1 strobe output. If unused, do not connect RX1_STROBE_OUT+.
N14	Output	RX1_STROBE_OUT-	In LVDS SSI mode, RX1_STROBE_OUT− is the Rx1 strobe output negative side. In CMOS SSI mode, RX1_STROBE_OUT− is not used. If unused, do not connect RX1_STROBE_OUT−.
P2	Input	TX2_STROBE_IN+	In LVDS SSI mode, TX2_STROBE_IN+ is the Tx2 strobe input positive side. In CMOS SSI mode, TX2_STROBE_IN+ is the Tx2 strobe input. If unused, do not connect TX2_STROBE_IN+.
P3	Input / Output	TX2_STROBE_IN-	In LVDS SSI mode, TX2_STROBE_IN− is the Tx2 strobe input negative side. In CMOS SSI mode, TX2_STROBE_IN − is the Tx2 reference data clock output. If unused, do not connect TX2_STROBE_IN−.
P4	Input	TX2_QDATA_IN−	In LVDS SSI mode, TX2_QDATA_IN− is the Tx2 Q sample data input negative side. In CMOS SSI mode, TX2_QDATA_IN− is the Tx2 Data Input 2. If unused, do not connect TX2_QDATA_IN−.
P5	Input	TX2_QDATA_IN+	In LVDS SSI mode, TX2_QDATA_IN+ is the Tx2 Q sample data input positive side. In CMOS SSI mode, TX2_QDATA_IN+ is the Tx2 Data Input 3. If unused, do not connect TX2_QDATA_IN+.
P6	Input	TX2_IDATA_IN+	In LVDS SSI mode, TX2_IDATA_IN+ is the Tx2 I sample data input positive side or the Tx2 I and Q sample data

			input positive side. In CMOS SSI mode, TX2_IDATA_IN+ is the Tx2 Data Input 1. If unused, do not connect TX2_IDATA_IN+.
P7	Input	TX2_IDATA_IN-	In LVDS SSI mode, TX2_IDATA_IN− is the Tx2 I sample data input negative side or the Tx2 I and Q sample data input negative side. In CMOS SSI mode, TX2_IDATA_IN− is the Tx2 Data Input 0 or the Tx2 I and Q sample data input. If unused, do not connect TX2_IDATA_IN−.
P8	Input	TX1_IDATA_IN−	In LVDS SSI mode, TX1_IDATA_IN− is the Tx1 I sample data input negative side or the Tx1 I and Q sample data input negative side. In CMOS SSI mode, TX1_IDATA_IN− is the Tx1 Data Input 0 or the Tx1 I and Q sample data input. If unused, do not connect TX1_IDATA_IN−.
P9	Input	TX1_IDATA_IN+	In LVDS SSI mode, TX1_IDATA_IN+ is the Tx1 I sample data input positive side or the Tx1 I and Q sample data input positive side. In CMOS SSI mode, TX1_IDATA_IN+ is the Tx1 Data Input 1. If unused, do not connect TX1_IDATA_IN+.
P10	Input	TX1_QDATA_IN+	In LVDS SSI mode, TX1_QDATA_IN+ is the Tx1 Q sample data input positive side. In CMOS SSI mode, TX1_QDATA_IN+ is the Tx1 Data Input 3. If unused, do not connect TX1_QDATA_IN+.
P11	Input	TX1_QDATA_IN-	In LVDS SSI mode, TX1_QDATA_IN− is the Tx1 Q sample data input negative side. In CMOS SSI mode, TX1_QDATA_IN− is the Tx1 Data Input 2. If unused, do not connect TX1_QDATA_IN−.
P12	Input / Output	TX1_STROBE_IN−	In LVDS SSI mode, TX1_STROBE_IN− is the Tx1 strobe input negative side. In CMOS SSI mode, TX1_STROBE_IN− is the Tx1 reference data clock output. If unused, do not connect TX1_STROBE_IN−.
P13	Input	TX1_STROBE_IN+	In LVDS SSI mode, TX1_STROBE_IN+ is the Tx1 strobe input positive side. In CMOS SSI mode, TX1_STROBE_IN+ is the Tx1 strobe input. If unused, do not connect TX1_STROBE_IN+.

Theory of Operation

The CBMRF9002 is a highly integrated RF transceiver that can be configured for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide transmit and receive functions in a single device. Programmability allows the two receiver channels and two transmitter channels to be used in TDD and FDD systems for mobile radio and cellular standards.

The CBMRF9002 contains serial interface links that consist of LVDS and a CMOS synchronous serial interface (CSSI). Both receiver and transmitter channels provide a low pin count and reliable data interface to a field-programmable gate array (FPGA) or other integrated baseband solutions.

The CBMRF9002 provides self calibration for dc offset, LO leakage, and QEC using an integrated microcontroller core to maintain a high performance level under varying temperatures and input signal conditions. Firmware is supplied with the device to schedule all calibrations with no user interaction.

- **Transmitter**

The CBMRF9002 uses a direct conversion transmitter architecture that consists of two identical and independently controlled channels that provide all digital processing, mixed signals, PLLs, and RF blocks necessary to implement a direct conversion system. Refer to Figure 4 for the transmitter data path overview.

The CBMRF9002 has an optional, fully programmable, 128-tap FIR. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each DAC has an adjustable sample rate and is linear up to full scale.

The DAC output produces baseband analog signals. The I and Q signals are first filtered to remove sampling artifacts and then fed to the upconversion mixers. At the mixer stage, the I and Q signals are recombined and modulated onto the carrier frequency for transmission to the output stage. Each transmit chain provides a wide attenuation adjustment range with fine granularity to help designers optimize the signal-to-noise ratio (SNR).

- **Receiver**

Figure 5 shows a simplified block diagram of the CBMRF9002 receiver. It is a fully integrated, direct conversion, low IF receiver signal chain. The receiver subsystem consists of a resistive input network for gain control followed by a current mode passive mixer. The output current of the mixer is converted to a voltage by a transimpedance amplifier and then digitized. There are two sets of ADCs, a high performance Σ-Δ ADC and a low power ADC. The digital baseband that provides the required filtering and decimation follows these ADCs.

There are two RF inputs for each receiver, and each input has independent IF downconversion path. RF inputs can switch between the two IF downconversion paths. The two downconversion paths can operate at different frequency,

To achieve gain control, a programmed gain index map is implemented. This gain map distributes attenuation among the various receiver blocks for optimal performance at each power level. The gain range is 30dB. Additional support is available for both automatic and manual gain control modes.

The receive LPFs can be reconfigured to help provide antialias filtering and improve out of band blockers. The CBMRF9002 is a wideband architecture transceiver that relies on the ADC high dynamic range to receive signals and interference at the same time. Filtering provided by the receive LPF attenuates ADC alias images. The receive LPF characteristic is flat and not intended to provide rejection of close in blockers. The baseband filter supports a baseband bandwidth from 5 MHz to 50MHz.

The receiver includes two ADC pairs. One pair consists of high performance Σ-Δ ADCs to provide maximum interferer tolerance, and the second pair consists of ADCs for significant power reduction. The extra pair of ADCs allow a smart trade-off between power and performance.

The ADC output can be conditioned further by a series of decimation filters and a fully programmable, 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block automatically adjusts with each change of the decimation factors to produce the desired output data rate.

For standards that demand low phase noise performance, the CBMRF9002 can operate in low IF mode. The CBMRF9002 can receive signals offset from the carrier, as with an IF downconversion scheme. A digital NCO and mixer that follow the analog receive path can downconvert the IF signal to baseband. Downconverting the signal to baseband allows a lower sample rate on the data bus. The CBMRF9002 makes no assumptions about high-side or low-side injection.

- **Observation Receiver**

The CBMRF9002 receiver signal chain can be configured to monitor the radio channel signal level in duty cycle detection and sleep fashion. Monitor mode allows the digital baseband processor to power down until the CBMRF9002 detects a signal. Monitor mode provides overall system power saving. The timing of detection and sleep mode is fully programmable. Alternatively, the CBMRF9002 can be under full control of the baseband processor during monitor mode.

- **Clock Input**

The reference clock inputs provide a low frequency clock from which all internal CBMRF9002 clocks are derived. The CBMRF9002 offers multiple reference input clocking options. The reference input clock pins on the device are labeled DEV_CLK_IN±. For optimal performance, drive the reference clock differentially via an external source or from an external crystal. If a differential input clock is provided, the clock signal must be ac-coupled with the input range limited from 10 MHz to 1 GHz. The CBMRF9002 can also accept an external crystal (XTAL) as a clock source. The frequency range of the supported crystal is between 20 MHz to 80 MHz. The external crystal connection must be dc-coupled. If a differential clock is not available, a single-ended, ac-coupled, 1 V p-p (maximum) CMOS signal can be applied to the DEV_CLK_IN+ pin with the DEV_CLK_IN− pin unconnected. The maximum clock frequency in this mode is limited to 80 MHz.

- **Frequency Synthesizer**

The CBMRF9002 offers two distinct PLL paths, an RF PLL for the high frequency RF path and a baseband PLL for the digital and sampling clocks of the data converters.

- **RF PLL**

The CBMRF9002 consists of five RF PLLs, main four PLLs (PLL1/2/3/4) support fast lock and fast frequency hopping. One auxiliary AuxPLL is used for calibration test. The four main PLLs can be configured flexibly for each of the receivers and transmitters. All the configurations are shown as table 7.

Mode	Specification	Configuration
1	4 PLLs for 4 channels	TX1A → PLL1 TX2A → PLL2 RX1A/B → PLL3 RX2A/B → PLL4
2	1 PLL for TX1 and RX1	TX1A & RX1A/B → PLL1 TX2A & RX2A/B → PLL2
3	1 PLL for TX1, RX1,TX2 and RX2 in fast frequency hopping application	TX1A & RX1A/B & TX2 & RX2A/B → PLL1

4	1 PLL for TX1 & TX2, 1 PLL for RX1 & RX2	TX1A & TX2A → PLL1 RX1A/B & RX2A/B → PLL2
5	External LO	EXT_LO1 → TX1A & RX1A/B EXT_LO2 → TX2A & RX2A/B

The RF PLL supports the use of both internal and external LO signals. The internal LO is generated by an on-chip VCO, which is tunable over a frequency range of 6.5 GHz to 14.5 GHz. The output of the VCO is phase-locked to an external reference clock through a fractional-N PLL that is programmable through the API command. The VCO outputs are steered through a combination of frequency dividers to produce in-phase and quadrature phase LO signals in the 10 MHz to 7.25 GHz frequency range.

Alternatively, an external LO signal can be applied to the external LO inputs of the CBMRF9002 to generate the LO signals in quadrature for the RF path. If the external LO path is chosen, the input frequency range is between 20 MHz and 14.5 GHz.

The CBMRF9002 supports various forms of fast frequency hopping (FFH) with the frequency dwell time and transition time as the main distinguishing factors between these forms. The RF PLL phase noise and the QEC and LOL algorithm performance degrade as a function of decreasing frequency transition times. FFH mode supports hop frequencies that are preloaded at power-up or streamed by the user onto the CBMRF9002. Hopping between the frequencies in FFH mode can be triggered by toggling a GPIO pin or executing an API command.

- **BB PLL**

The CBMRF9002 contains a baseband PLL synthesizer that generates all baseband and data port related clocks. The clocks can be used for high speed ADC, DAC，digital baseband signal processing unit and MCU. The clocks can be programmed based on the system frequency and sample rate.

- **SPI**

The CBMRF9002 uses an SPI to communicate with the baseband processor. This interface can be configured either as a 4-wire interface with dedicated receive and transmit ports, or as a 3-wire interface with a bidirectional data communications port. This bus allows the baseband processor to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 32-bit format. The first bit sets the bus direction of the bus transfer. The next 31 bits set the address where the data is written. The next 32 bits contain the data transferred to the specific register address. And the data can be written continuously with the address added automatically. More than 8 SPI_CLKs should be transferred following the last 32 bits data for proper write operation.

Read commands follow a similar format without the more than 8 SPI_CLKs.

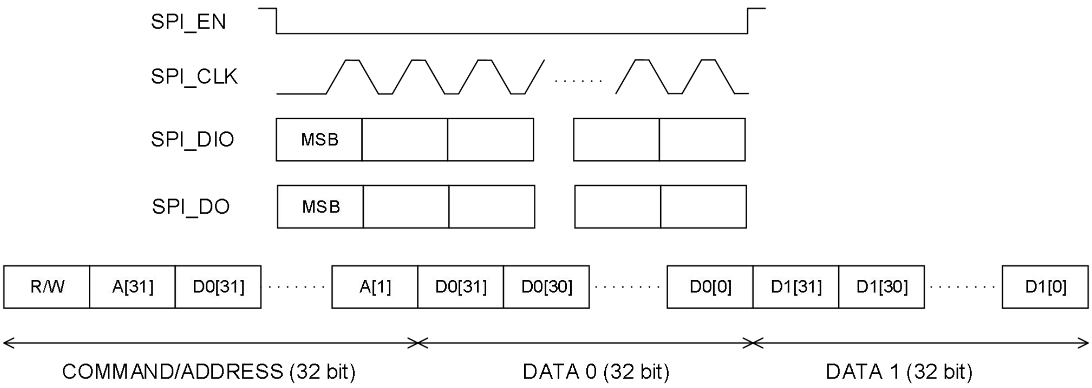

Figure 4 SPI Timming

- **Digital GPIO**

The CBMRF9002 GPIO signals referenced to the VDIGIO_1P8 supply are intended to interface with digital circuitry and can be configured for numerous functions. Some of these pins, when configured as outputs, are used by the baseband processor as real-time signals to provide a number of internal settings and measurements. This configuration allows the baseband processor to monitor receiver performance in different situations. Signals used for manual gain mode, calibration flags, state machine states, and various receiver parameters are among the outputs that can be monitored on these pins. In addition, certain pins can be configured as inputs and used in various functions, such as setting the receiver gain or transmitter attenuation in real time.

- **Analog GPIO**

The AGPIO pins are intended to interface with system blocks that perform analog functions. The AGPIO pins referenced to the VAGPIO_1P8 supply provide control signals to the external components, such as the low noise amplifier (LNA) or digital step attenuator (DSA). The selected AGPIO pins provide an alternate auxiliary DAC functionality.

- **Auxiliary ADC Inputs**

The CBMRF9002 contains four auxiliary ADCs with the corresponding inputs connected to four dedicated input pins (AUXADC_x). This block can monitor system voltages without additional components. The auxiliary ADC is 12 bits with an input voltage range of 0.05 V to VDDA_1P8 –

0.05V. When enabled, the auxiliary ADC is free running. An API function allows the user to read back the last value latched by the ADC.

- **Auxiliary DAC outputs**

The CBMRF9002 contains four identical auxiliary DACs (AUXDAC_x) that can supply bias voltages, analog control voltages, or other system functionality. The auxiliary DACs (AUXDAC_0 to AUXDAC_3) are multiplexed with the AGPIO_xx pins. The auxiliary DACs are 10 bits and have an output voltage range of approximately 0.05 V to VDDA_1P8 – 0.05 V and have a current drive of 10 mA. The auxiliary DACs generate ramp up and ramp down patterns that can be loaded into the CBMRF9002 and then triggered based on state of dedicated DGPIO pin.

- **Digital interface CSSI/LSSI**

The CBMRF9002 data interface supports both CMOS and LVDS electrical interfaces. The data bus width can be 24-bit, 16-bit and 12-bit in MSB mode. In CMOS mode, the interface supports 1-lane and 4-lane operation with maximum lane rate 491.52 Mbps. In 1-lane configuration, the data transferred on lane 0, I data before Q data. In 4-lane configuration, I data are on lane 0 and lane 1, Q data on lane 2 and lane 3. In LVDS mode, the interface supports 1-lane and 2-lane DDR operation with maximum lane rate 983.04 Mbps. In 1-lane configuration, the data transferred on lane 0, I data before Q data. In 2-lane configuration, I data are on lane 0, Q data on lane 1.

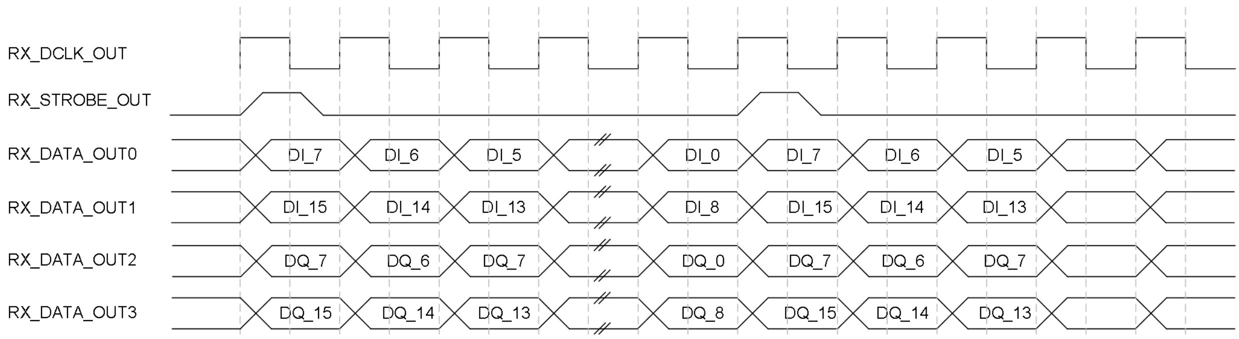

Figure 5 CSSI 4-Line Mode

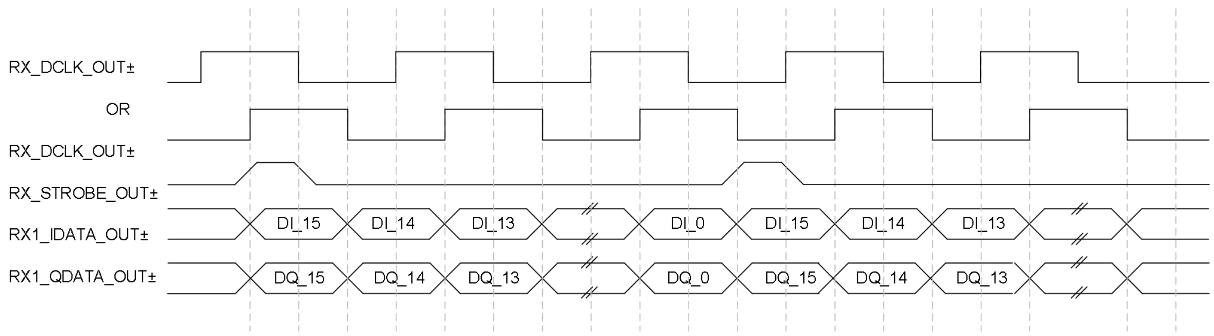

Figure 6 LSSI 2-Line Mode

Table 8 and table 9 illustrate the relationship of lane configuration and lane rate.

In 24-bit mode, the actual data resolution is 18-bit.

Table 8

CSSI lane	Data width/bit	Lane Rate/Mbps	Signal Width/Mhz
1	16	15.36	12.5
1	24	10.24	8.5
4	12	81.92	70
4	16	61.44	50
4	24	40.96	34

Table 9

LSSI lane	Data width/bit	Lane Rate/Mbps	Signal Width/Mhz
1	16	30.72	25
1	24	20.48	17
2	12	81.92	70
2	16	61.44	50
2	24	40.96	34

Outline Dimensions

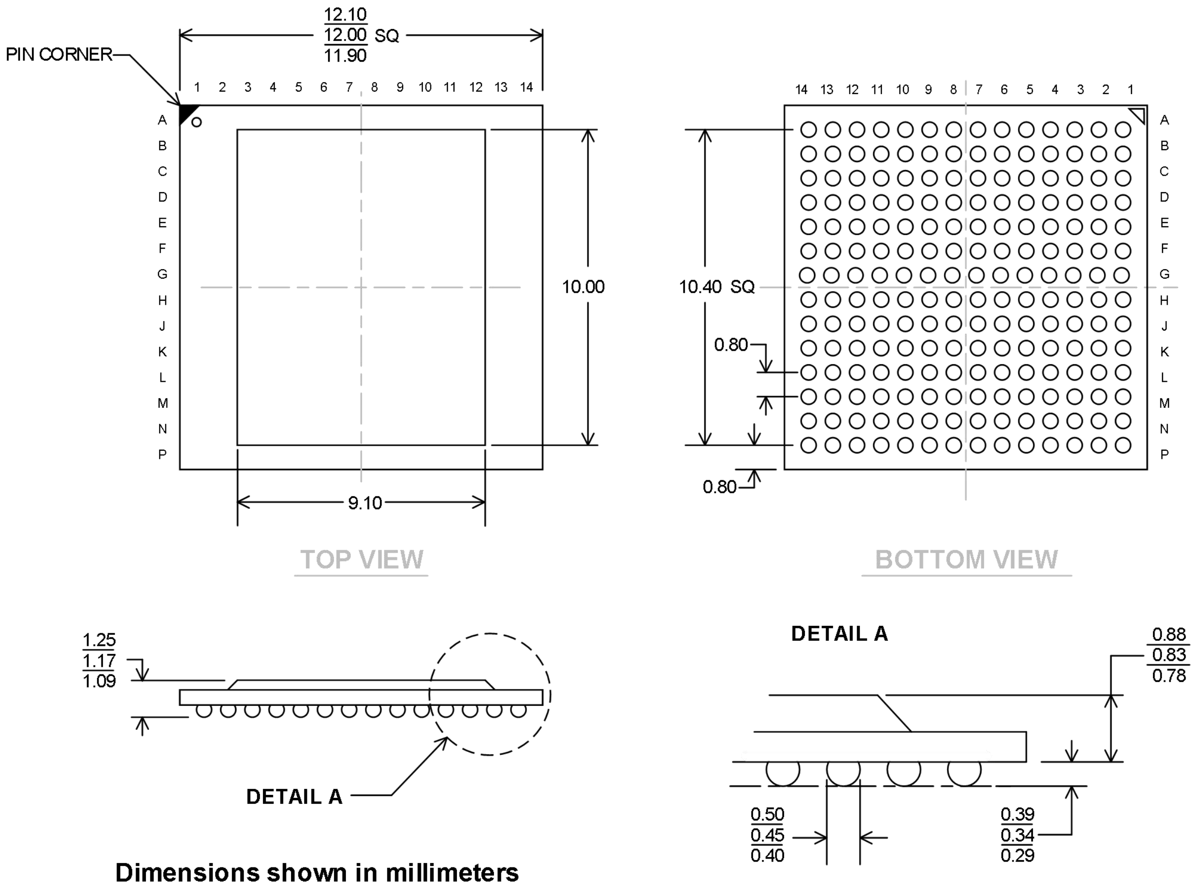

Figure 6 196-Ball Flip Chip Ball Grid Array

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION	MAKING INFORMATION
CBMRF9002BG		-40℃~85℃	CSP_BGA 196		